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ILI9806E-2C

a-Si TFT LCD Single-Chip Driver 480(RGB)x864 Resolution, 16.7M-color Without internal GRAM

Data Sheet

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Introduction

The ILI9806E-2C is a 16.7M single-chip SOC driver for a-Si TFT liquid crystal display panels with a resolution up to 480(RGB)x864. The ILI9806E-2C is comprised of a 1441-channel source driver, an gate-IC-less level shifter, and a power supply circuit.

The ILI9806E-2C supports 3-line serial peripheral interface to input commands. The ILI9806E-2C supports a RGB (16-/18-/24-bit) data bus for video image display. For high-speed serial interface, the MIPI DSI interface mode, the ILI9806E-2C supports two data lanes and one clock lane for high-speed and low power transmission in both directions with low EMI noise.

The ILI9806E-2C operates a wide range of an analog power supplies. The ILI9806E-2C supports sleep mode and deep standby power management functions, making the ILI9806E-2C an ideal LCD driver for medium or small sized portable products such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics display where conserving battery power is desired. Additionally, it has an internal DC/DC converter that generates the LCD driving voltage and the voltage follower circuit for LCD driver.

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1. Features

- Display resolution options:
  - 480(RGB) (H) X 864 (V)
  - 480(RGB) (H) X 854 (V)
  - 480(RGB) (H) X 800 (V)
  - 480(RGB) (H) X 720 (V)
  - 480(RGB) (H) X 640 (V)

- Display color modes
  - Full color mode:

    16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
  - Reduced color modes:

    262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)

    65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)

- Display module
  - Supports 1441 source channel outputs
  - Supports gate control signals to gate driver in the panel
  - Supports 2-dot / column inversion
  - Gamma correction (1 preset Gamma curve)
  - On module VCOM control (DDVDL+0.3V to 0V common electrode output voltage range)

- Interface types
  - MIPI-DSI (Display Serial Interface) interface

    Supports one data lane / maximum speed 850Mbps or

    Supports two data lanes / maximum speed 500Mbps

    Supports DSI version 1.02.00

    Supports D-PHY version 1.00.00

    Supports DCS version 1.02.00
  - MIPI-DPI (Display Pixel Interface) interface

    16 bit/pixel (R: 5-bit, G: 6-bit, B: 5-bit)

    18 bit/pixel (R: 6-bit, G: 6-bit, B: 6-bit)

    24 bit/pixel (R: 8-bit, G: 8-bit, B: 8-bit)
  - 3 line-9bit SPI (Serial Peripheral Interface) interface

- Power saving mode:
  - Deep-standby mode
  - Sleep mode

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- Other on-chip functions / Miscellaneous
  - Supports inversion mode
  - Software programmable color depth mode
  - Supports DC VCOM driving
  - DC VCOM voltage generator and adjustment
  - OTP (One-Time Programming) memory store initialization register settings
  - Provide 3 times OTP to store DC VCOM value setting, ID setting
  - Supports CABC (Content Adaptive Brightness Control) function
  - Separate RGB Gamma correction
  - Supports 3-Gamma DGC (Digital Gamma Correction) function
  - Color enhancement function
  - Supports control the ILI4002 and ILI4003 IC
  - VGHO/VGLO voltage generator for gate control signal in panel
  - Supports gate control signals to gate driver in panel (GIP)

- Input power
  - I/O supply voltage range for IOVCC to DGND = 1.65V ~ 3.6V
  - Analog supply voltage range for VCI/VCIR/VCIP to AGND/DGND/CGND/VSSR1/VSSR2/VSSR3 = 2.5V ~ 3.6V
  - OTP programming voltage, VPP = 5.0V

- Source/VCOM/Gate power supply voltage
  - DDVDH-AGND=4.75 to 6.5V (Step-up 1 output voltage range)
  - DDVDL-AGND = -6.5 to -4.75V (Step-up 2 output voltage range)
  - VCL-AGND = -1 X VCIP (Step-up 3 output voltage range)
  - DC VCOM = -4.0V to 0V, a step 12.5mV (Common electrode voltage range)
  - VREG1OUT= 3.0V to 6.1875V (DDVDH-0.3V) (Positive gamma high voltage range)
  - VREG2OUT= -3.0V to -6.1875V (DDVDL+0.3V) (Negative gamma high voltage range)
  - VGH-AGND = 8.0V to 18.0V (Positive gate driver output voltage range)
  - VGL-AGND = -8.0V to -18.0V (Negative gate driver output voltage range)
  - VGL_REG-AGND = -7.0 to -15.5V (Negative gate driver output voltage range)
  - VGH_REG-AGND = 8.5V to 16.0V (Positive gate driver output voltage range)

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2. Device Overview

2.1. Block Diagram

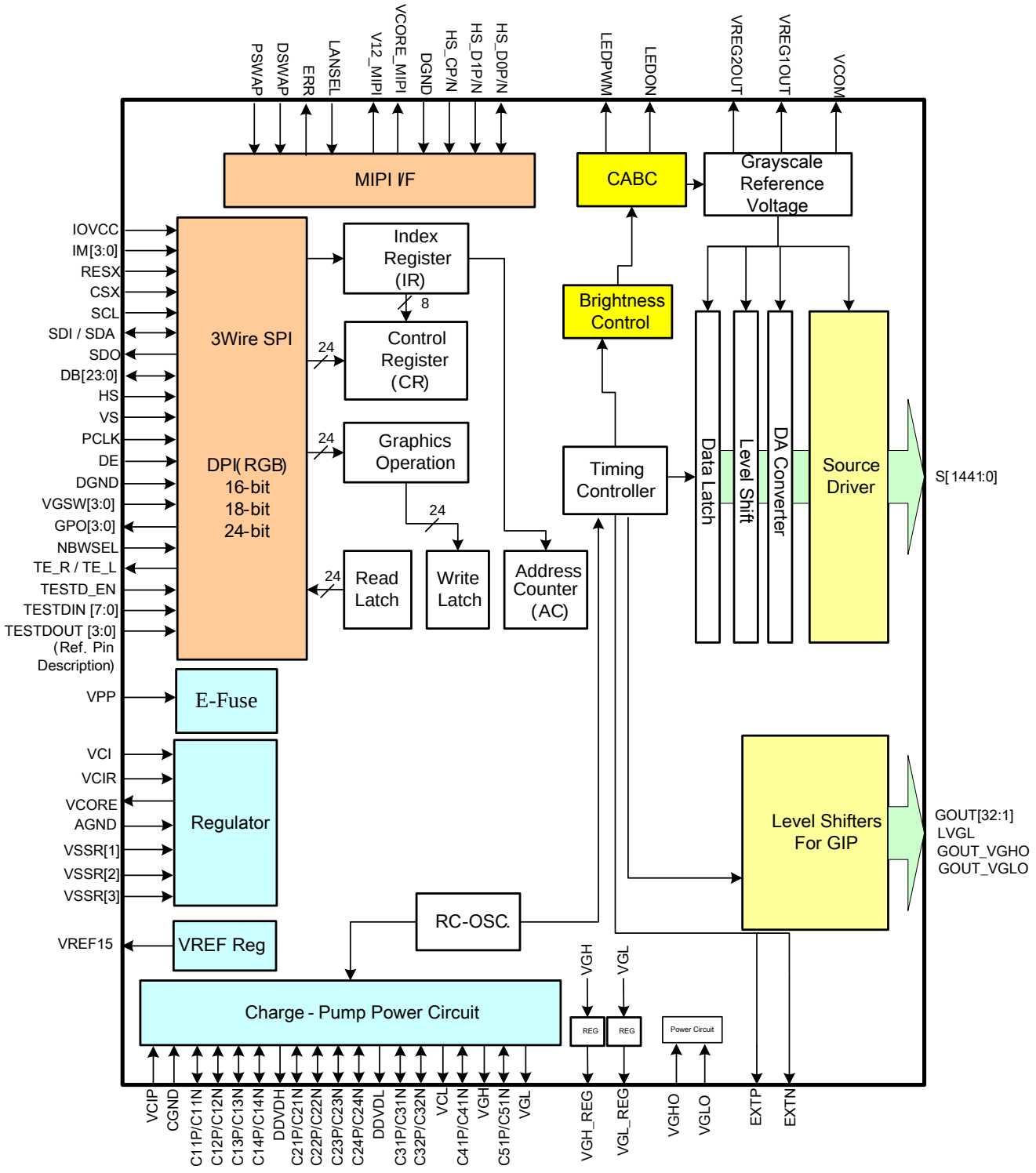


Figure 1 Block Diagram

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2.2. Block Function Description

2.2.1. System Interface

The interface operating mode (DPI or DSI) is selected by hardware pins IM [3:0], see Table 1 below.

Table 1 System Operating Mode [Note 1]

IM3	IM2	IM1	IM0	Interface	IO Pin in Use
0	0	1	1	DPI with SPI (3-line 9-bit)	DB[23:0] ,VS, HS, DE, PCLK, SDI,SDO,SCL(rising edge),CSX
1	0	0	1		
1	0	1	0		
1	0	1	1		DB[23:0] , VS, HS, DE, PCLK, SDI,SDO,SCL(falling edge),CSX
0	1	0	1	MIPI DSI Interface	HS_D0P,HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN
0	1	1	1	MIPI DSI Interface+SPI (When set IM[3:0]=0111, the SPI I/F only supports the CABC function (command 51h~56h, 5Eh, 5Fh), and the others command are prohibited.)	HS_D0P,HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN,SDI,SDO,SCL(rising edge) ,CSX
1	1	1	1	MIPI DSI Interface+SPI (When set IM[3:0]=1111, the SPI I/F only supports the CABC function (command 51h~56h, 5Eh, 5Fh), and the others command are prohibited.)	HS_D0P,HS_D0N, HS_D1P, HS_D1N, HS_CP, HS_CN, SDI,SDO,SCL(falling edge) ,CSX

2.2.2. Parallel RGB Interface

The DPI (RGB) interface is used as the external interface for displaying moving pictures. When the DPI (RGB) interface is selected, display operations are synchronized with the externally supplied signals, VS, HS, and PCLK. In DPI (RGB) interface mode, data (DB[23:0]) are written in synchronization with these signals according to the polarity of the DE signal (Data Enable); this is done in order to prevent flicker on the display while updating display data.

2.2.3. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates the LCD drive voltage which corresponds to 256 grayscale level set in the Gamma correction register. The ILI9806E-2C can display up to 16.7M colors at the maximum.

2.2.4. Timing Generating

The timing generator is used to generate timing signals for operating internal circuits.

2.2.5. Oscillator

The ILI9806E-2C incorporates an RC oscillator circuit. Command settings are used to change the frame frequency.

Note 1 Set Number of Set number of colors using set pixel format: 3Ah.

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2.2.6. Source Driver Circuit

The LCD display driver circuit consists of a 480-output source driver (S0~S1441). The display pattern data is latched when 480RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

2.2.7. Panel Control Circuit

The panel control circuit outputs GOUT [32:1] signals at either VGH, VGL, VGH_REG, VGL_REG, LVGL level.

2.2.8. Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to register setting.

2.2.9. MIPI DSI Controller Circuit

The MIPI DSI controller circuit consists of the D-PHY controller, Protocol Control Unit (PCU), Packet Processing Unit (PPU), ECC generating circuit, internal data/command buffer and analog transceiver. The D-PHY controls communication with the analog block and the ECC generating circuit generates the ECC to check the outgoing data stream for accuracy of the receiving data packet. The PCU controls outgoing and incoming data streams and the PPU controls transmitting packet distribution and merging. The internal data and command buffer is used for temporary storage of incoming command and display data.

2.2.10. CABC (Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

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2.3. Pin Descriptions

Table 2 Bus Interface Pins

<table>
<tr><th colspan="3">Bus Interface Pins</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>-Select the interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td rowspan="3">DPI with SPI 3-line (SCL rising edge)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>DPI with SPI 3-line (SCL falling edge)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>MIPI DSI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>MIPI DSI+SPI (SCL rising edge)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>MIPI DSI+SPI (SCL falling edge)</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>- The external reset input.
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>CSX</td><td>I</td><td>-A chip select signal.
Low: the chip is selected and accessible
High: the chip is not selected and not accessible
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>SCL</td><td>I</td><td>- The SPI Interface (SCL): Serves as a write signal and writes data at the rising edge.
- Serial interface (SCL): Serial clock input.
Fix to IOVCC or DGND level when not in use.</td></tr>
<tr><td>DB[23:0]</td><td>I/O</td><td>- A 24-bit parallel bi-directional data bus for DPI (RGB) I/F
Fix to IOVCC , DGND level or Open when not in use</td></tr>
<tr><td>SDI
(SDA)</td><td>I/O</td><td>Serial data input pin used for the SPI Interface.
SDI : Serial data input pin
SDA : Serial data input/output bidirectional pin
Fix to IOVCC or DGND level when not in use</td></tr>
<tr><td>SDO</td><td>O</td><td>Serial data output pin used for the SPI Interface.
Leave the pin to open when not in use.</td></tr>
<tr><td>TE_L / TE_R</td><td>O</td><td>-Tearing effect output
TE_L= TE_R
Leave the pin to open when not in use.</td></tr>
<tr><td>PCLK</td><td>I</td><td>- Dot clock signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>VS</td><td>I</td><td>- Frame synchronizing signal for DPI (RGB) interface operation.
Fix to DGND level when not in use.</td></tr>
<tr><td>HS</td><td>I</td><td>- Line synchronizing signal for DPI (RGB) interface operation.</td></tr>
</table>

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<table>
<tr><td></td><td></td><td>Fix to DGND level when not in use.</td></tr>
<tr><td>DE</td><td>I</td><td>- Data enable signal for DPI (RGB) interface operation.
Low : access enabled.
High : access inhibited.
Fix to DGND level when not in use.</td></tr>
<tr><td>HS_CP
HS_CN</td><td>I</td><td>MIPI DSI differential clock pair (DSI-CLK+/-).
If MIPI are not used, they should be connected to DGND.</td></tr>
<tr><td>HS_D0P
HS_D0N
HS_D1P
HS_D1N</td><td>I/O</td><td>MIPI DSI differential data pair (DSI-Dn+/-).
If MIPI are not used, they should be connected to DGND</td></tr>
<tr><td>ERR</td><td>O</td><td>- CRC and ECC error output pin for MIPI interface, activated by S/W command. This pin is output low when it is not activated. When this pin is activated, it output high if CRC/ECC error found.
Leave the pin to open when not in use.</td></tr>
<tr><td>LANSEL</td><td>I</td><td>- Input pin to select 1 data lane or 2 data lanes in MIPI interface.
Low: 1 data lane.
High: 2 data lanes.
- The pin have internal pull low resister.
Fix to DGND level when not in use.</td></tr>
<tr><td>DSWAP
PSWAP</td><td>I</td><td>- Differential clock polarity swap
For MIPI DSI interface
<table>
<tr><th>DSWAP</th><th>PSWAP</th><th>Original Order</th><th>HS_D1P</th><th>HS_D1N</th><th>HS_CP</th><th>HS_CN</th><th>HS_D0P</th><th>HS_D0N</th></tr>
<tr><td>0</td><td>0</td><td>Afer Swap</td><td>HS_D1P</td><td>HS_D1N</td><td>HS_CP</td><td>HS_CN</td><td>HS_D0P</td><td>HS_D0N</td></tr>
<tr><td>0</td><td>1</td><td>Afer Swap</td><td>HS_D1N</td><td>HS_D1P</td><td>HS_CN</td><td>HS_CP</td><td>HS_D0N</td><td>HS_D0P</td></tr>
<tr><td>1</td><td>0</td><td>Afer Swap</td><td>HS_D0P</td><td>HS_D0N</td><td>HS_CP</td><td>HS_CN</td><td>HS_D1P</td><td>HS_D1N</td></tr>
<tr><td>1</td><td>1</td><td>Afer Swap</td><td>HS_D0N</td><td>HS_D0P</td><td>HS_CN</td><td>HS_CP</td><td>HS_D1N</td><td>HS_D1P</td></tr>
</table>
Fix to DGND level when not in use.</td></tr>
<tr><td>NBWSEL</td><td>I</td><td>- Input pin to select the gamma voltage level sequence of V0~V255.
Low: V0>V1>…>V254>V255, normally white.
High: V255>V254>…>V1>V0, normally black.
Fix to DGND level when not in use.</td></tr>
<tr><td>VGSW[3:0]</td><td>I</td><td>- Input pin to select the different application.
- The pins have internal pull-low resister.
Leave the pin to open when not in use.</td></tr>
<tr><td>GPO[3:0]</td><td>O</td><td>- General purpose output pins.
Leave the pin to open when not in use.</td></tr>
<tr><td>LEDON</td><td>O</td><td>- Used for turning On/Off external LED backlight control.
Leave the pin to open when not in use.</td></tr>
<tr><td>LEDPWM</td><td>O</td><td>- The PWM frequency output for LED driver control.
Leave the pin to open when not in use.</td></tr>
</table>

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Table 3 Driver Output Pins

Driver Output Pins		
Pin Name	I/O	Descriptions
S[0:1441]	O	- Source output voltage signals applied to a LCD panel.
GOUT[1:32]	O	- Gate control signals and the swing voltage level is VGHO to VGLO.
GOUT_VGHO	O	- High voltage level for GIP control signals and gate circuit of panel.
GOUT_VGLO	O	- Low voltage level for GIP control signals and gate circuit of panel.
VGHO	O	- High voltage level for GIP control signals and gate circuit of panel.
VGLO	O	- Low voltage level for GIP control signals and gate circuit of panel.
LVGL	O	- Low voltage level for gate circuit of panel.
VCOM	O	- Regulator output for common voltage of panel.
DMY_VSS	O	- Dummy Source. ***Leave the pin to open when not in use.***

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Table 4 Charge Pump Relative Pins

Charge Pump Relative Pins		
Pin Name	I/O	Descriptions
DDVDH	O	- Output voltage from step-up circuit 1, generated from VCI. - Connect to a stabilizing capacitor between DDVDH and AGND.
DDVDL	O	- Output voltage from step-up circuit 2, generated from VCI. - Connect to a stabilizing capacitor between DDVDL and AGND.
VCL	O	- Output voltage from step-up circuit 3, generated from VCI. - Connect to a stabilizing capacitor between VCL and AGND.
VGH	O	- Output voltage from step-up circuit 4, generated from VCI. - Connect to a stabilizing capacitor between VGH and AGND.
VGL	O	- Output voltage from step-up circuit 5, generated from VCI. - Connect to a stabilizing capacitor between VGL and AGND.
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	-	- Connect the charge-pumping capacitor for generating DDVDH level. - Capacitor connection pins for the step-up circuit 1.
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	-	- Connect the charge-pumping capacitor for generating DDVDLlevel. - Capacitor connection pins for the step-up circuit 2.
C31P, C31N C32P, C32N	-	- Connect the charge-pumping capacitor for generating VCL level. - Capacitor connection pins for the step-up circuit 3.
C41P, C41N	-	- Connect the charge-pumping capacitor for generating VGH level. - Capacitor connection pins for the step-up circuit 4.
C51P, C51N	-	- Connect the charge-pumping capacitor for generating VGL level. - Capacitor connection pins for the step-up circuit 5.

Table 5 ILI4002 and ILI4003 Control Pins

ILI4002 and ILI4003 Control Pins		
Pin Name	I/O	Descriptions
EXTP (CTRL_A)	O	-CTRL_A : Control signal for a external charge pump IC (ex: ILI4002 or ILI4003) - The level voltage is between VCI and GND.
EXTN (CTRL_B)	O	-CTRL_B : Control signal for a external charge pump IC (ex: ILI4002 or ILI4003) - The level voltage is between VCI and GND.

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Table 6 Power Pins

Power Pins		
Pin Name	I/O	Descriptions
VCI	P	- Power supply for analog system. - VCI, VCIR and VCIP should be the same input voltage level of 2.5 ~ 3.6V.
VCIR	P	- Power supply for regulator low voltage reference circuit. - VCI, VCIR and VCIP should be the same input voltage level of 2.5 ~ 3.6V.
VCIP	P	- Power supply for DC/DC converter. - VCI, VCIR and VCIP should be the same input voltage level of 2.5 ~ 3.6V.
IOVCC	P	- Power supply for I/O block. ***Excluded MIPI interface.***
VCORE	O	- internal logic voltage output - Connect a capacitor for stabilization.
VGH_REG	O	- Output voltage generated from VGH. - Connect a capacitor for stabilization. ***Leave the pin to open when not in use.***
VGL_REG	O	- Output voltage generated from VGL. LDO output used for panel voltage. - Connect a capacitor for stabilization. ***Leave the pin to open when not in use.***
VREF15	O	- Regulator output voltage for power voltage. - Connect a capacitor for stabilization.
VREG1OUT	O	- Output voltage generated from DDVDH. LDO output for positive gamma voltage generator.
VREG2OUT	O	- Output voltage generated from DDVDL. LDO output for negative gamma voltage generator.
VCORE_MIPI	O	- Regulator output for internal MIPI DSI analog system (1.5V typical) - Connect a capacitor for stabilization.
V12_MIPI	O	- Regulator output for internal MIPI DSI low power system (1.2V typical) - Connect a capacitor for stabilization.
AGND	P	- System ground for analog circuit.
CGND	P	- System ground for DC/DC convertor.
DGND	P	- System ground for internal digital system.
VSSR[1] VSSR[2] VSSR[3]	P	- System ground for regulator low voltage reference circuit.
VPP	I	- OTP programming power. ***Fix to DGND level when not in use.***

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Table 7 Test Pins

Test Pins		
Pin Name	I/O	Descriptions
PADA[1:4] PADB[1:4]	I/O	- These test pins for chip attachment detection. - PADA[1:4] are output pins and PADB[1:4] are input pins - For normal operation: Connect PADA1 and PADB1 together by ITO trace. Connect PADA2 and PADB2 together by ITO trace. Connect PADA3 and PADB3 together by ITO trace. Connect PADA4 and PADB4 together by ITO trace.
CONTACT1A CONTACT2A CONTACT1B CONTACT2B	I/O	- Test pin, for test bonding quality, IC internal connect CONTACT1A , CONTACT1B, CONTACT2A with CONTACT2B
TESTD_EN	I/O	- Test pin, It is not accessible to user. must be open. - This pin have internal pull low resister.
TESTDIN[7:0]	-	- Test pin, It is not accessible to user. must be open. - This pin have internal pull low resister.
TESTDOUT[3:0]	-	- Test pin, It is not accessible to user. must be open.
DMY	-	- These pins are dummy (Non-function inside).

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2.4. Pin assignment

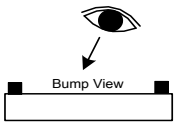
Chip Size: 24000 um x 800 um

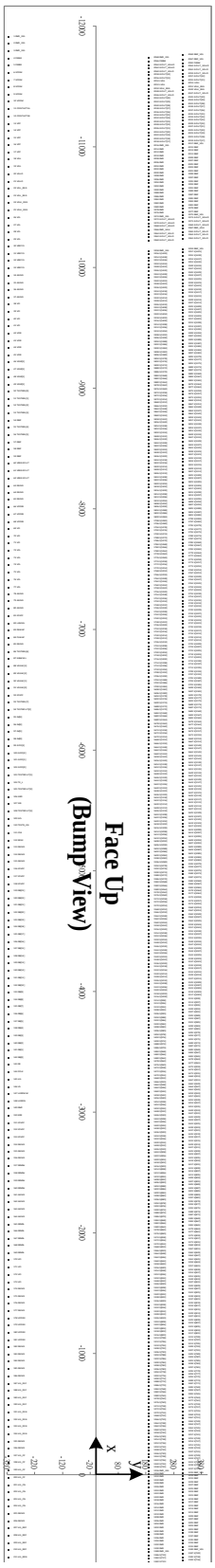
Pad Location : Pad Center.

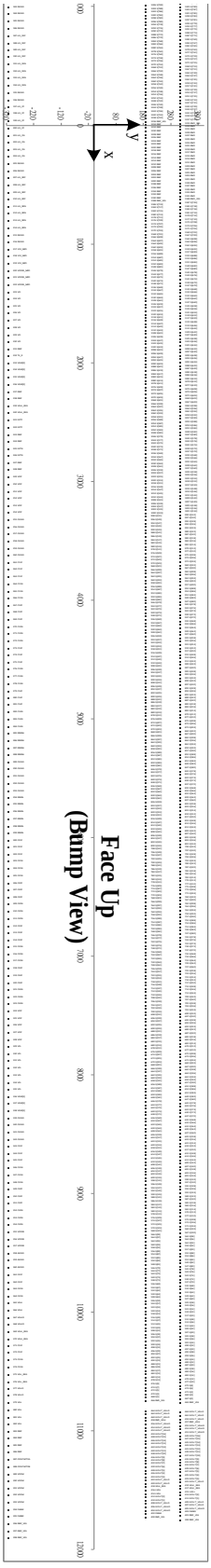
Coordinate Origin : Chip center

Bump Size:

1. Input Side : 40um x 90um
2. Output Side : 14um x 95um

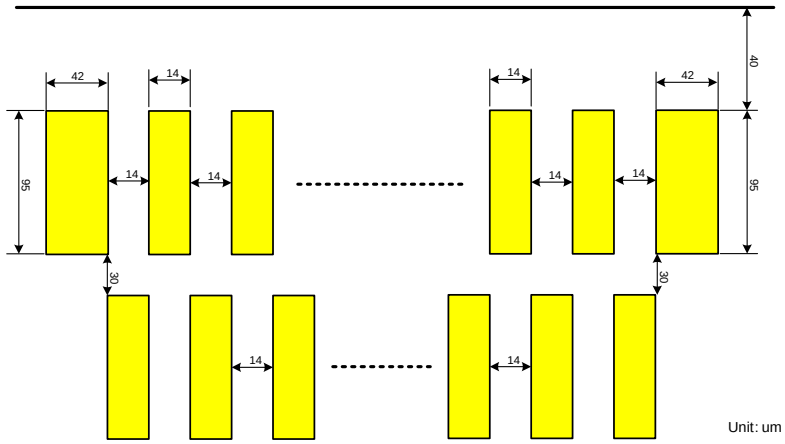
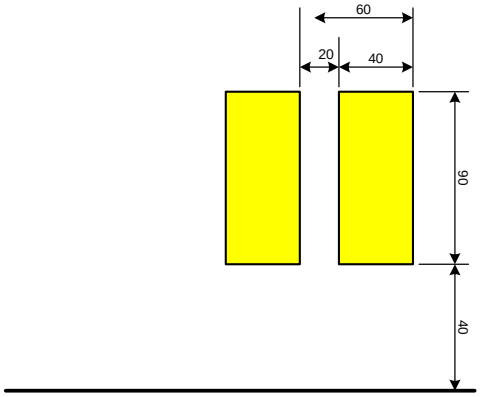
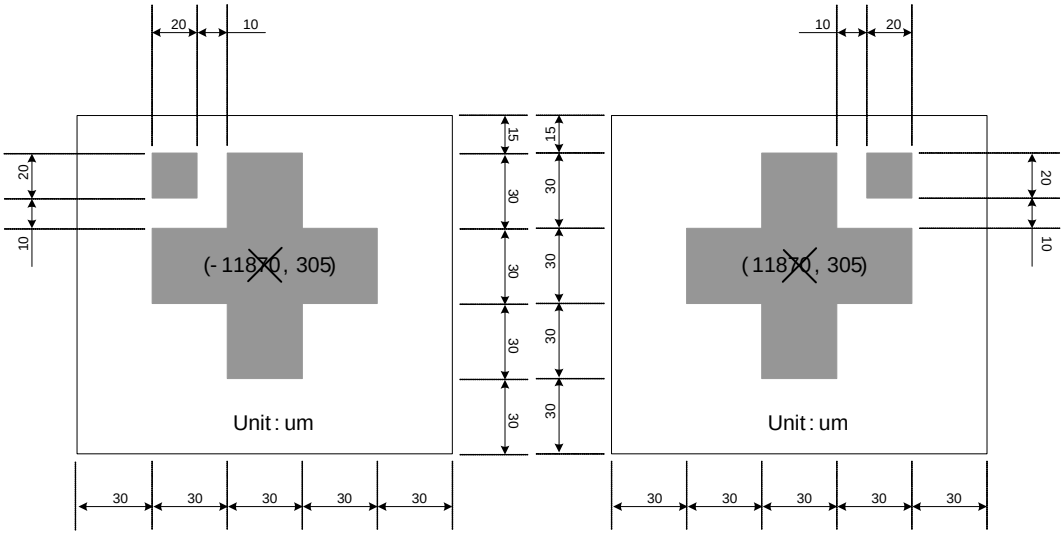






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2.5. Bump Arrangement

Output PAD	
Input PAD	
Alignment mark	

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2.6. Pad Coordination

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1	DMY_VSS	-11910	-315	61	VREG2OUT	-8310	-315	121	DB[21]	-4710	-315	181	VCORE	-1110	-315
2	DMY_VSS	-11850	-315	62	VREG1OUT	-8250	-315	122	DB[20]	-4650	-315	182	DGND	-1050	-315
3	DMY_VSS	-11790	-315	63	DGND	-8190	-315	123	DB[19]	-4590	-315	183	DGND	-990	-315
4	PADA1	-11730	-315	64	DGND	-8130	-315	124	DB[18]	-4530	-315	184	DGND	-930	-315
5	PADB1	-11670	-315	65	DGND	-8070	-315	125	DB[17]	-4470	-315	185	DGND	-870	-315
6	VCOM	-11610	-315	66	VCORE	-8010	-315	126	DB[16]	-4410	-315	186	DGND	-810	-315
7	VCOM	-11550	-315	67	VCORE	-7950	-315	127	DB[15]	-4350	-315	187	HS_D1P	-750	-315
8	VCOM	-11490	-315	68	VCORE	-7890	-315	128	DB[14]	-4290	-315	188	HS_D1P	-690	-315
9	VCOM	-11430	-315	69	VCI	-7830	-315	129	DB[13]	-4230	-315	189	HS_D1P	-630	-315
10	VCOM	-11370	-315	70	VCI	-7770	-315	130	DB[12]	-4170	-315	190	HS_D1P	-570	-315
11	CONTACT1A	-11310	-315	71	VCI	-7710	-315	131	DB[11]	-4110	-315	191	HS_D1N	-510	-315
12	CONTACT1B	-11250	-315	72	VCL	-7650	-315	132	DB[10]	-4050	-315	192	HS_D1N	-450	-315
13	VPP	-11190	-315	73	VCL	-7590	-315	133	DB[9]	-3990	-315	193	HS_D1N	-390	-315
14	VPP	-11130	-315	74	VCL	-7530	-315	134	DB[8]	-3930	-315	194	HS_D1N	-330	-315
15	VPP	-11070	-315	75	VCL	-7470	-315	135	DB[7]	-3870	-315	195	DGND	-270	-315
16	VPP	-11010	-315	76	VCL	-7410	-315	136	DB[6]	-3810	-315	196	DGND	-210	-315
17	VPP	-10950	-315	77	VCL	-7350	-315	137	DB[5]	-3750	-315	197	HS_CP	-150	-315
18	VGL	-10890	-315	78	AGND	-7290	-315	138	DB[4]	-3690	-315	198	HS_CP	-90	-315
19	VGL	-10830	-315	79	AGND	-7230	-315	139	DB[3]	-3630	-315	199	HS_CP	-30	-315
20	VGLO	-10770	-315	80	AGND	-7170	-315	140	DB[2]	-3570	-315	200	HS_CP	30	-315
21	VGLO	-10710	-315	81	IOVCC	-7110	-315	141	DB[1]	-3510	-315	201	HS_CN	90	-315
22	VGL_REG	-10650	-315	82	LANSEL	-7050	-315	142	DB[0]	-3450	-315	202	HS_CN	150	-315
23	VGL_REG	-10590	-315	83	DSWAP	-6990	-315	143	DE	-3390	-315	203	HS_CN	210	-315
24	VGH_REG	-10530	-315	84	PSWAP	-6930	-315	144	PCLK	-3330	-315	204	HS_CN	270	-315
25	VGH_REG	-10470	-315	85	DGND	-6870	-315	145	HS	-3270	-315	205	DGND	330	-315
26	VCL	-10410	-315	86	TESTDIN[6]	-6810	-315	146	VS	-3210	-315	206	DGND	390	-315
27	VCL	-10350	-315	87	NBWSEL	-6750	-315	147	LEDPWM	-3150	-315	207	HS_D0P	450	-315
28	VCL	-10290	-315	88	VGSW[3]	-6690	-315	148	LEDON	-3090	-315	208	HS_D0P	510	-315
29	VCL	-10230	-315	89	VGSW[2]	-6630	-315	149	DMY	-3030	-315	209	HS_D0P	570	-315
30	VREF15	-10170	-315	90	VGSW[1]	-6570	-315	150	ERR	-2970	-315	210	HS_D0P	630	-315
31	VREF15	-10110	-315	91	VGSW[0]	-6510	-315	151	IOVCC	-2910	-315	211	HS_D0N	690	-315
32	VREF15	-10050	-315	92	IOVCC	-6450	-315	152	IOVCC	-2850	-315	212	HS_D0N	750	-315
33	VREF15	-9990	-315	93	TESTDIN[7]	-6390	-315	153	IOVCC	-2790	-315	213	HS_D0N	810	-315
34	AGND	-9930	-315	94	TESTDOUT[0]	-6330	-315	154	DGND	-2730	-315	214	HS_D0N	870	-315
35	AGND	-9870	-315	95	IM[3]	-6270	-315	155	DGND	-2670	-315	215	DGND	930	-315
36	AGND	-9810	-315	96	IM[2]	-6210	-315	156	DGND	-2610	-315	216	DGND	990	-315
37	AGND	-9750	-315	97	IM[1]	-6150	-315	157	DDVDH	-2550	-315	217	V12_MIPI	1050	-315
38	VCI	-9690	-315	98	IM[0]	-6090	-315	158	DDVDH	-2490	-315	218	V12_MIPI	1110	-315
39	VCI	-9630	-315	99	GPO[3]	-6030	-315	159	DDVDH	-2430	-315	219	V12_MIPI	1170	-315
40	VCI	-9570	-315	100	GPO[2]	-5970	-315	160	DDVDH	-2370	-315	220	VCORE_MIPI	1230	-315
41	VCI	-9510	-315	101	GPO[1]	-5910	-315	161	AGND	-2310	-315	221	VCORE_MIPI	1290	-315
42	VCIR	-9450	-315	102	GPO[0]	-5850	-315	162	AGND	-2250	-315	222	VCORE_MIPI	1350	-315
43	VCIR	-9390	-315	103	TESTDOUT[1]	-5790	-315	163	AGND	-2190	-315	223	VCI	1410	-315
44	VCIR	-9330	-315	104	TE_L	-5730	-315	164	AGND	-2130	-315	224	VCI	1470	-315
45	VCIR	-9270	-315	105	TESTDOUT[2]	-5670	-315	165	DDVDL	-2070	-315	225	VCI	1530	-315
46	VSSR[1]	-9210	-315	106	SDO	-5610	-315	166	DDVDL	-2010	-315	226	VCI	1590	-315
47	VSSR[1]	-9150	-315	107	SDI	-5550	-315	167	DDVDL	-1950	-315	227	VCI	1650	-315
48	VSSR[1]	-9090	-315	108	TESTDOUT[3]	-5490	-315	168	DDVDL	-1890	-315	228	VCI	1710	-315
49	VSSR[1]	-9030	-315	109	SCL	-5430	-315	169	DDVDL	-1830	-315	229	VCI	1770	-315
50	TESTDIN[0]	-8970	-315	110	TESTD_EN	-5370	-315	170	VCI	-1770	-315	230	VCI	1830	-315
51	TESTDIN[1]	-8910	-315	111	CSX	-5310	-315	171	VCI	-1710	-315	231	DMY	1890	-315
52	TESTDIN[2]	-8850	-315	112	RESX	-5250	-315	172	VCI	-1650	-315	232	TE_R	1950	-315
53	TESTDIN[3]	-8790	-315	113	DGND	-5190	-315	173	VCI	-1590	-315	233	VSSR[2]	2010	-315
54	DMY	-8730	-315	114	DGND	-5130	-315	174	DGND	-1530	-315	234	VSSR[2]	2070	-315
55	TESTDIN[4]	-8670	-315	115	DGND	-5070	-315	175	DGND	-1470	-315	235	VSSR[2]	2130	-315
56	TESTDIN[5]	-8610	-315	116	IOVCC	-5010	-315	176	DGND	-1410	-315	236	VSSR[2]	2190	-315
57	DMY	-8550	-315	117	IOVCC	-4950	-315	177	DGND	-1350	-315	237	DMY	2250	-315
58	DMY	-8490	-315	118	IOVCC	-4890	-315	178	VCORE	-1290	-315	238	DMY	2310	-315
59	DMY	-8430	-315	119	DB[23]	-4830	-315	179	VCORE	-1230	-315	239	VGH_REG	2370	-315
60	VREG2OUT	-8370	-315	120	DB[22]	-4770	-315	180	VCORE	-1170	-315	240	VGH_REG	2430	-315

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
241	EXTP	2490	-315	301	C21P	6090	-315	361	C41P	9690	-315	421	GOUT_VGLO	11438	312.5
242	EXTP	2550	-315	302	C21P	6150	-315	362	C41P	9750	-315	422	GOUT_VGLO	11424	187.5
243	DMY	2610	-315	303	C21N	6210	-315	363	C41N	9810	-315	423	GOUT[3]	11410	312.5
244	DMY	2670	-315	304	C21N	6270	-315	364	C41N	9870	-315	424	GOUT[3]	11396	187.5
245	EXTN	2730	-315	305	C21N	6330	-315	365	VGH	9930	-315	425	GOUT[4]	11382	312.5
246	EXTN	2790	-315	306	C22P	6390	-315	366	VGH	9990	-315	426	GOUT[4]	11368	187.5
247	DMY	2850	-315	307	C22P	6450	-315	367	VGHO	10050	-315	427	GOUT[5]	11354	312.5
248	DMY	2910	-315	308	C22P	6510	-315	368	VGHO	10110	-315	428	GOUT[5]	11340	187.5
249	VCIP	2970	-315	309	C22N	6570	-315	369	VGH_REG	10170	-315	429	GOUT[6]	11326	312.5
250	VCIP	3030	-315	310	C22N	6630	-315	370	VGH_REG	10230	-315	430	GOUT[6]	11312	187.5
251	VCIP	3090	-315	311	C22N	6690	-315	371	C51P	10290	-315	431	GOUT[7]	11298	312.5
252	VCIP	3150	-315	312	C23P	6750	-315	372	C51P	10350	-315	432	GOUT[7]	11284	187.5
253	VCIP	3210	-315	313	C23P	6810	-315	373	C51N	10410	-315	433	GOUT[8]	11270	312.5
254	VCIP	3270	-315	314	C23P	6870	-315	374	C51N	10470	-315	434	GOUT[8]	11256	187.5
255	CGND	3330	-315	315	C23N	6930	-315	375	VGL_REG	10530	-315	435	GOUT[9]	11242	312.5
256	CGND	3390	-315	316	C23N	6990	-315	376	VGL_REG	10590	-315	436	GOUT[9]	11228	187.5
257	CGND	3450	-315	317	C23N	7050	-315	377	VGLO	10650	-315	437	GOUT[10]	11214	312.5
258	CGND	3510	-315	318	C24P	7110	-315	378	VGLO	10710	-315	438	GOUT[10]	11200	187.5
259	CGND	3570	-315	319	C24P	7170	-315	379	VGL	10770	-315	439	GOUT[11]	11186	312.5
260	CGND	3630	-315	320	C24P	7230	-315	380	VGL	10830	-315	440	GOUT[11]	11172	187.5
261	C11P	3690	-315	321	C24N	7290	-315	381	VGL	10890	-315	441	GOUT[12]	11158	312.5
262	C11P	3750	-315	322	C24N	7350	-315	382	VGL	10950	-315	442	GOUT[12]	11144	187.5
263	C11P	3810	-315	323	C24N	7410	-315	383	DMY	11010	-315	443	GOUT[13]	11130	312.5
264	C11N	3870	-315	324	VCIP	7470	-315	384	DMY	11070	-315	444	GOUT[13]	11116	187.5
265	C11N	3930	-315	325	VCIP	7530	-315	385	DMY	11130	-315	445	GOUT[14]	11102	312.5
266	C11N	3990	-315	326	VCIP	7590	-315	386	DMY	11190	-315	446	GOUT[14]	11088	187.5
267	C12P	4050	-315	327	VCIP	7650	-315	387	CONTACT2A	11250	-315	447	GOUT[15]	11074	312.5
268	C12P	4110	-315	328	VCIP	7710	-315	388	CONTACT2B	11310	-315	448	GOUT[15]	11060	187.5
269	C12P	4170	-315	329	VCL	7770	-315	389	VCOM	11370	-315	449	GOUT[16]	11046	312.5
270	C12N	4230	-315	330	VCL	7830	-315	390	VCOM	11430	-315	450	GOUT[16]	11032	187.5
271	C12N	4290	-315	331	VCL	7890	-315	391	VCOM	11490	-315	451	GOUT_VGHO	11018	312.5
272	C12N	4350	-315	332	VCL	7950	-315	392	VCOM	11550	-315	452	GOUT_VGHO	11004	187.5
273	C13P	4410	-315	333	VCL	8010	-315	393	VCOM	11610	-315	453	GOUT_VGHO	10990	312.5
274	C13P	4470	-315	334	VCL	8070	-315	394	PADA2	11670	-315	454	GOUT_VGHO	10976	187.5
275	C13P	4530	-315	335	VCL	8130	-315	395	PADB2	11730	-315	455	GOUT_VGHO	10962	312.5
276	C13N	4590	-315	336	VSSR[3]	8190	-315	396	DMY_VSS	11790	-315	456	GOUT_VGHO	10948	187.5
277	C13N	4650	-315	337	VSSR[3]	8250	-315	397	DMY_VSS	11850	-315	457	DMY_VGH	10934	312.5
278	C13N	4710	-315	338	VSSR[3]	8310	-315	398	DMY_VSS	11910	-315	458	DMY_VGH	10920	187.5
279	C14P	4770	-315	339	CGND	8370	-315	399	DMY_VSS	11760	312.5	459	GOUT_VGLO	10906	312.5
280	C14P	4830	-315	340	CGND	8430	-315	400	DMY_VSS	11732	187.5	460	GOUT_VGLO	10892	187.5
281	C14P	4890	-315	341	CGND	8490	-315	401	DMY_VSS	11718	312.5	461	GOUT_VGLO	10878	312.5
282	C14N	4950	-315	342	CGND	8550	-315	402	PADA3	11704	187.5	462	GOUT_VGLO	10864	187.5
283	C14N	5010	-315	343	C31P	8610	-315	403	PADB3	11690	312.5	463	GOUT_VGLO	10850	312.5
284	C14N	5070	-315	344	C31P	8670	-315	404	GOUT_VGHO	11676	187.5	464	GOUT_VGLO	10836	187.5
285	DDVDH	5130	-315	345	C31P	8730	-315	405	GOUT_VGHO	11662	312.5	465	DMY_VSS	10766	312.5
286	DDVDH	5190	-315	346	C31N	8790	-315	406	GOUT_VGHO	11648	187.5	466	DMY_VSS	10752	187.5
287	DDVDH	5250	-315	347	C31N	8850	-315	407	GOUT_VGLO	11634	312.5	467	S[0]	10738	312.5
288	DDVDH	5310	-315	348	C31N	8910	-315	408	GOUT_VGLO	11620	187.5	468	S[1]	10724	187.5
289	CGND	5370	-315	349	C32P	8970	-315	409	GOUT_VGLO	11606	312.5	469	S[2]	10710	312.5
290	CGND	5430	-315	350	C32P	9030	-315	410	GOUT[1]	11592	187.5	470	S[3]	10696	187.5
291	CGND	5490	-315	351	C32P	9090	-315	411	GOUT[1]	11578	312.5	471	S[4]	10682	312.5
292	CGND	5550	-315	352	C32N	9150	-315	412	GOUT[2]	11564	187.5	472	S[5]	10668	187.5
293	CGND	5610	-315	353	C32N	9210	-315	413	GOUT[2]	11550	312.5	473	S[6]	10654	312.5
294	DDVDL	5670	-315	354	C32N	9270	-315	414	LVGL	11536	187.5	474	S[7]	10640	187.5
295	DDVDL	5730	-315	355	VCORE	9330	-315	415	LVGL	11522	312.5	475	S[8]	10626	312.5
296	DDVDL	5790	-315	356	VCORE	9390	-315	416	LVGL	11508	187.5	476	S[9]	10612	187.5
297	DDVDL	5850	-315	357	VCORE	9450	-315	417	VGH_REG	11494	312.5	477	S[10]	10598	312.5
298	DDVDL	5910	-315	358	AGND	9510	-315	418	VGH_REG	11480	187.5	478	S[11]	10584	187.5
299	DDVDL	5970	-315	359	AGND	9570	-315	419	VGH_REG	11466	312.5	479	S[12]	10570	312.5
300	C21P	6030	-315	360	AGND	9630	-315	420	GOUT_VGLO	11452	187.5	480	S[13]	10556	187.5

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
481	S[14]	10542	312.5	541	S[74]	9702	312.5	601	S[134]	8862	312.5	661	S[194]	8022	312.5
482	S[15]	10528	187.5	542	S[75]	9688	187.5	602	S[135]	8848	187.5	662	S[195]	8008	187.5
483	S[16]	10514	312.5	543	S[76]	9674	312.5	603	S[136]	8834	312.5	663	S[196]	7994	312.5
484	S[17]	10500	187.5	544	S[77]	9660	187.5	604	S[137]	8820	187.5	664	S[197]	7980	187.5
485	S[18]	10486	312.5	545	S[78]	9646	312.5	605	S[138]	8806	312.5	665	S[198]	7966	312.5
486	S[19]	10472	187.5	546	S[79]	9632	187.5	606	S[139]	8792	187.5	666	S[199]	7952	187.5
487	S[20]	10458	312.5	547	S[80]	9618	312.5	607	S[140]	8778	312.5	667	S[200]	7938	312.5
488	S[21]	10444	187.5	548	S[81]	9604	187.5	608	S[141]	8764	187.5	668	S[201]	7924	187.5
489	S[22]	10430	312.5	549	S[82]	9590	312.5	609	S[142]	8750	312.5	669	S[202]	7910	312.5
490	S[23]	10416	187.5	550	S[83]	9576	187.5	610	S[143]	8736	187.5	670	S[203]	7896	187.5
491	S[24]	10402	312.5	551	S[84]	9562	312.5	611	S[144]	8722	312.5	671	S[204]	7882	312.5
492	S[25]	10388	187.5	552	S[85]	9548	187.5	612	S[145]	8708	187.5	672	S[205]	7868	187.5
493	S[26]	10374	312.5	553	S[86]	9534	312.5	613	S[146]	8694	312.5	673	S[206]	7854	312.5
494	S[27]	10360	187.5	554	S[87]	9520	187.5	614	S[147]	8680	187.5	674	S[207]	7840	187.5
495	S[28]	10346	312.5	555	S[88]	9506	312.5	615	S[148]	8666	312.5	675	S[208]	7826	312.5
496	S[29]	10332	187.5	556	S[89]	9492	187.5	616	S[149]	8652	187.5	676	S[209]	7812	187.5
497	S[30]	10318	312.5	557	S[90]	9478	312.5	617	S[150]	8638	312.5	677	S[210]	7798	312.5
498	S[31]	10304	187.5	558	S[91]	9464	187.5	618	S[151]	8624	187.5	678	S[211]	7784	187.5
499	S[32]	10290	312.5	559	S[92]	9450	312.5	619	S[152]	8610	312.5	679	S[212]	7770	312.5
500	S[33]	10276	187.5	560	S[93]	9436	187.5	620	S[153]	8596	187.5	680	S[213]	7756	187.5
501	S[34]	10262	312.5	561	S[94]	9422	312.5	621	S[154]	8582	312.5	681	S[214]	7742	312.5
502	S[35]	10248	187.5	562	S[95]	9408	187.5	622	S[155]	8568	187.5	682	S[215]	7728	187.5
503	S[36]	10234	312.5	563	S[96]	9394	312.5	623	S[156]	8554	312.5	683	S[216]	7714	312.5
504	S[37]	10220	187.5	564	S[97]	9380	187.5	624	S[157]	8540	187.5	684	S[217]	7700	187.5
505	S[38]	10206	312.5	565	S[98]	9366	312.5	625	S[158]	8526	312.5	685	S[218]	7686	312.5
506	S[39]	10192	187.5	566	S[99]	9352	187.5	626	S[159]	8512	187.5	686	S[219]	7672	187.5
507	S[40]	10178	312.5	567	S[100]	9338	312.5	627	S[160]	8498	312.5	687	S[220]	7658	312.5
508	S[41]	10164	187.5	568	S[101]	9324	187.5	628	S[161]	8484	187.5	688	S[221]	7644	187.5
509	S[42]	10150	312.5	569	S[102]	9310	312.5	629	S[162]	8470	312.5	689	S[222]	7630	312.5
510	S[43]	10136	187.5	570	S[103]	9296	187.5	630	S[163]	8456	187.5	690	S[223]	7616	187.5
511	S[44]	10122	312.5	571	S[104]	9282	312.5	631	S[164]	8442	312.5	691	S[224]	7602	312.5
512	S[45]	10108	187.5	572	S[105]	9268	187.5	632	S[165]	8428	187.5	692	S[225]	7588	187.5
513	S[46]	10094	312.5	573	S[106]	9254	312.5	633	S[166]	8414	312.5	693	S[226]	7574	312.5
514	S[47]	10080	187.5	574	S[107]	9240	187.5	634	S[167]	8400	187.5	694	S[227]	7560	187.5
515	S[48]	10066	312.5	575	S[108]	9226	312.5	635	S[168]	8386	312.5	695	S[228]	7546	312.5
516	S[49]	10052	187.5	576	S[109]	9212	187.5	636	S[169]	8372	187.5	696	S[229]	7532	187.5
517	S[50]	10038	312.5	577	S[110]	9198	312.5	637	S[170]	8358	312.5	697	S[230]	7518	312.5
518	S[51]	10024	187.5	578	S[111]	9184	187.5	638	S[171]	8344	187.5	698	S[231]	7504	187.5
519	S[52]	10010	312.5	579	S[112]	9170	312.5	639	S[172]	8330	312.5	699	S[232]	7490	312.5
520	S[53]	9996	187.5	580	S[113]	9156	187.5	640	S[173]	8316	187.5	700	S[233]	7476	187.5
521	S[54]	9982	312.5	581	S[114]	9142	312.5	641	S[174]	8302	312.5	701	S[234]	7462	312.5
522	S[55]	9968	187.5	582	S[115]	9128	187.5	642	S[175]	8288	187.5	702	S[235]	7448	187.5
523	S[56]	9954	312.5	583	S[116]	9114	312.5	643	S[176]	8274	312.5	703	S[236]	7434	312.5
524	S[57]	9940	187.5	584	S[117]	9100	187.5	644	S[177]	8260	187.5	704	S[237]	7420	187.5
525	S[58]	9926	312.5	585	S[118]	9086	312.5	645	S[178]	8246	312.5	705	S[238]	7406	312.5
526	S[59]	9912	187.5	586	S[119]	9072	187.5	646	S[179]	8232	187.5	706	S[239]	7392	187.5
527	S[60]	9898	312.5	587	S[120]	9058	312.5	647	S[180]	8218	312.5	707	S[240]	7378	312.5
528	S[61]	9884	187.5	588	S[121]	9044	187.5	648	S[181]	8204	187.5	708	S[241]	7364	187.5
529	S[62]	9870	312.5	589	S[122]	9030	312.5	649	S[182]	8190	312.5	709	S[242]	7350	312.5
530	S[63]	9856	187.5	590	S[123]	9016	187.5	650	S[183]	8176	187.5	710	S[243]	7336	187.5
531	S[64]	9842	312.5	591	S[124]	9002	312.5	651	S[184]	8162	312.5	711	S[244]	7322	312.5
532	S[65]	9828	187.5	592	S[125]	8988	187.5	652	S[185]	8148	187.5	712	S[245]	7308	187.5
533	S[66]	9814	312.5	593	S[126]	8974	312.5	653	S[186]	8134	312.5	713	S[246]	7294	312.5
534	S[67]	9800	187.5	594	S[127]	8960	187.5	654	S[187]	8120	187.5	714	S[247]	7280	187.5
535	S[68]	9786	312.5	595	S[128]	8946	312.5	655	S[188]	8106	312.5	715	S[248]	7266	312.5
536	S[69]	9772	187.5	596	S[129]	8932	187.5	656	S[189]	8092	187.5	716	S[249]	7252	187.5
537	S[70]	9758	312.5	597	S[130]	8918	312.5	657	S[190]	8078	312.5	717	S[250]	7238	312.5
538	S[71]	9744	187.5	598	S[131]	8904	187.5	658	S[191]	8064	187.5	718	S[251]	7224	187.5
539	S[72]	9730	312.5	599	S[132]	8890	312.5	659	S[192]	8050	312.5	719	S[252]	7210	312.5
540	S[73]	9716	187.5	600	S[133]	8876	187.5	660	S[193]	8036	187.5	720	S[253]	7196	187.5

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
721	S[254]	7182	312.5	781	S[314]	6342	312.5	841	S[374]	5502	312.5	901	S[434]	4662	312.5
722	S[255]	7168	187.5	782	S[315]	6328	187.5	842	S[375]	5488	187.5	902	S[435]	4648	187.5
723	S[256]	7154	312.5	783	S[316]	6314	312.5	843	S[376]	5474	312.5	903	S[436]	4634	312.5
724	S[257]	7140	187.5	784	S[317]	6300	187.5	844	S[377]	5460	187.5	904	S[437]	4620	187.5
725	S[258]	7126	312.5	785	S[318]	6286	312.5	845	S[378]	5446	312.5	905	S[438]	4606	312.5
726	S[259]	7112	187.5	786	S[319]	6272	187.5	846	S[379]	5432	187.5	906	S[439]	4592	187.5
727	S[260]	7098	312.5	787	S[320]	6258	312.5	847	S[380]	5418	312.5	907	S[440]	4578	312.5
728	S[261]	7084	187.5	788	S[321]	6244	187.5	848	S[381]	5404	187.5	908	S[441]	4564	187.5
729	S[262]	7070	312.5	789	S[322]	6230	312.5	849	S[382]	5390	312.5	909	S[442]	4550	312.5
730	S[263]	7056	187.5	790	S[323]	6216	187.5	850	S[383]	5376	187.5	910	S[443]	4536	187.5
731	S[264]	7042	312.5	791	S[324]	6202	312.5	851	S[384]	5362	312.5	911	S[444]	4522	312.5
732	S[265]	7028	187.5	792	S[325]	6188	187.5	852	S[385]	5348	187.5	912	S[445]	4508	187.5
733	S[266]	7014	312.5	793	S[326]	6174	312.5	853	S[386]	5334	312.5	913	S[446]	4494	312.5
734	S[267]	7000	187.5	794	S[327]	6160	187.5	854	S[387]	5320	187.5	914	S[447]	4480	187.5
735	S[268]	6986	312.5	795	S[328]	6146	312.5	855	S[388]	5306	312.5	915	S[448]	4466	312.5
736	S[269]	6972	187.5	796	S[329]	6132	187.5	856	S[389]	5292	187.5	916	S[449]	4452	187.5
737	S[270]	6958	312.5	797	S[330]	6118	312.5	857	S[390]	5278	312.5	917	S[450]	4438	312.5
738	S[271]	6944	187.5	798	S[331]	6104	187.5	858	S[391]	5264	187.5	918	S[451]	4424	187.5
739	S[272]	6930	312.5	799	S[332]	6090	312.5	859	S[392]	5250	312.5	919	S[452]	4410	312.5
740	S[273]	6916	187.5	800	S[333]	6076	187.5	860	S[393]	5236	187.5	920	S[453]	4396	187.5
741	S[274]	6902	312.5	801	S[334]	6062	312.5	861	S[394]	5222	312.5	921	S[454]	4382	312.5
742	S[275]	6888	187.5	802	S[335]	6048	187.5	862	S[395]	5208	187.5	922	S[455]	4368	187.5
743	S[276]	6874	312.5	803	S[336]	6034	312.5	863	S[396]	5194	312.5	923	S[456]	4354	312.5
744	S[277]	6860	187.5	804	S[337]	6020	187.5	864	S[397]	5180	187.5	924	S[457]	4340	187.5
745	S[278]	6846	312.5	805	S[338]	6006	312.5	865	S[398]	5166	312.5	925	S[458]	4326	312.5
746	S[279]	6832	187.5	806	S[339]	5992	187.5	866	S[399]	5152	187.5	926	S[459]	4312	187.5
747	S[280]	6818	312.5	807	S[340]	5978	312.5	867	S[400]	5138	312.5	927	S[460]	4298	312.5
748	S[281]	6804	187.5	808	S[341]	5964	187.5	868	S[401]	5124	187.5	928	S[461]	4284	187.5
749	S[282]	6790	312.5	809	S[342]	5950	312.5	869	S[402]	5110	312.5	929	S[462]	4270	312.5
750	S[283]	6776	187.5	810	S[343]	5936	187.5	870	S[403]	5096	187.5	930	S[463]	4256	187.5
751	S[284]	6762	312.5	811	S[344]	5922	312.5	871	S[404]	5082	312.5	931	S[464]	4242	312.5
752	S[285]	6748	187.5	812	S[345]	5908	187.5	872	S[405]	5068	187.5	932	S[465]	4228	187.5
753	S[286]	6734	312.5	813	S[346]	5894	312.5	873	S[406]	5054	312.5	933	S[466]	4214	312.5
754	S[287]	6720	187.5	814	S[347]	5880	187.5	874	S[407]	5040	187.5	934	S[467]	4200	187.5
755	S[288]	6706	312.5	815	S[348]	5866	312.5	875	S[408]	5026	312.5	935	S[468]	4186	312.5
756	S[289]	6692	187.5	816	S[349]	5852	187.5	876	S[409]	5012	187.5	936	S[469]	4172	187.5
757	S[290]	6678	312.5	817	S[350]	5838	312.5	877	S[410]	4998	312.5	937	S[470]	4158	312.5
758	S[291]	6664	187.5	818	S[351]	5824	187.5	878	S[411]	4984	187.5	938	S[471]	4144	187.5
759	S[292]	6650	312.5	819	S[352]	5810	312.5	879	S[412]	4970	312.5	939	S[472]	4130	312.5
760	S[293]	6636	187.5	820	S[353]	5796	187.5	880	S[413]	4956	187.5	940	S[473]	4116	187.5
761	S[294]	6622	312.5	821	S[354]	5782	312.5	881	S[414]	4942	312.5	941	S[474]	4102	312.5
762	S[295]	6608	187.5	822	S[355]	5768	187.5	882	S[415]	4928	187.5	942	S[475]	4088	187.5
763	S[296]	6594	312.5	823	S[356]	5754	312.5	883	S[416]	4914	312.5	943	S[476]	4074	312.5
764	S[297]	6580	187.5	824	S[357]	5740	187.5	884	S[417]	4900	187.5	944	S[477]	4060	187.5
765	S[298]	6566	312.5	825	S[358]	5726	312.5	885	S[418]	4886	312.5	945	S[478]	4046	312.5
766	S[299]	6552	187.5	826	S[359]	5712	187.5	886	S[419]	4872	187.5	946	S[479]	4032	187.5
767	S[300]	6538	312.5	827	S[360]	5698	312.5	887	S[420]	4858	312.5	947	S[480]	4018	312.5
768	S[301]	6524	187.5	828	S[361]	5684	187.5	888	S[421]	4844	187.5	948	S[481]	4004	187.5
769	S[302]	6510	312.5	829	S[362]	5670	312.5	889	S[422]	4830	312.5	949	S[482]	3990	312.5
770	S[303]	6496	187.5	830	S[363]	5656	187.5	890	S[423]	4816	187.5	950	S[483]	3976	187.5
771	S[304]	6482	312.5	831	S[364]	5642	312.5	891	S[424]	4802	312.5	951	S[484]	3962	312.5
772	S[305]	6468	187.5	832	S[365]	5628	187.5	892	S[425]	4788	187.5	952	S[485]	3948	187.5
773	S[306]	6454	312.5	833	S[366]	5614	312.5	893	S[426]	4774	312.5	953	S[486]	3934	312.5
774	S[307]	6440	187.5	834	S[367]	5600	187.5	894	S[427]	4760	187.5	954	S[487]	3920	187.5
775	S[308]	6426	312.5	835	S[368]	5586	312.5	895	S[428]	4746	312.5	955	S[488]	3906	312.5
776	S[309]	6412	187.5	836	S[369]	5572	187.5	896	S[429]	4732	187.5	956	S[489]	3892	187.5
777	S[310]	6398	312.5	837	S[370]	5558	312.5	897	S[430]	4718	312.5	957	S[490]	3878	312.5
778	S[311]	6384	187.5	838	S[371]	5544	187.5	898	S[431]	4704	187.5	958	S[491]	3864	187.5
779	S[312]	6370	312.5	839	S[372]	5530	312.5	899	S[432]	4690	312.5	959	S[492]	3850	312.5
780	S[313]	6356	187.5	840	S[373]	5516	187.5	900	S[433]	4676	187.5	960	S[493]	3836	187.5

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
961	S[494]	3822	312.5	1021	S[554]	2982	312.5	1081	S[614]	2142	312.5	1141	S[674]	1302	312.5
962	S[495]	3808	187.5	1022	S[555]	2968	187.5	1082	S[615]	2128	187.5	1142	S[675]	1288	187.5
963	S[496]	3794	312.5	1023	S[556]	2954	312.5	1083	S[616]	2114	312.5	1143	S[676]	1274	312.5
964	S[497]	3780	187.5	1024	S[557]	2940	187.5	1084	S[617]	2100	187.5	1144	S[677]	1260	187.5
965	S[498]	3766	312.5	1025	S[558]	2926	312.5	1085	S[618]	2086	312.5	1145	S[678]	1246	312.5
966	S[499]	3752	187.5	1026	S[559]	2912	187.5	1086	S[619]	2072	187.5	1146	S[679]	1232	187.5
967	S[500]	3738	312.5	1027	S[560]	2898	312.5	1087	S[620]	2058	312.5	1147	S[680]	1218	312.5
968	S[501]	3724	187.5	1028	S[561]	2884	187.5	1088	S[621]	2044	187.5	1148	S[681]	1204	187.5
969	S[502]	3710	312.5	1029	S[562]	2870	312.5	1089	S[622]	2030	312.5	1149	S[682]	1190	312.5
970	S[503]	3696	187.5	1030	S[563]	2856	187.5	1090	S[623]	2016	187.5	1150	S[683]	1176	187.5
971	S[504]	3682	312.5	1031	S[564]	2842	312.5	1091	S[624]	2002	312.5	1151	S[684]	1162	312.5
972	S[505]	3668	187.5	1032	S[565]	2828	187.5	1092	S[625]	1988	187.5	1152	S[685]	1148	187.5
973	S[506]	3654	312.5	1033	S[566]	2814	312.5	1093	S[626]	1974	312.5	1153	S[686]	1134	312.5
974	S[507]	3640	187.5	1034	S[567]	2800	187.5	1094	S[627]	1960	187.5	1154	S[687]	1120	187.5
975	S[508]	3626	312.5	1035	S[568]	2786	312.5	1095	S[628]	1946	312.5	1155	S[688]	1106	312.5
976	S[509]	3612	187.5	1036	S[569]	2772	187.5	1096	S[629]	1932	187.5	1156	S[689]	1092	187.5
977	S[510]	3598	312.5	1037	S[570]	2758	312.5	1097	S[630]	1918	312.5	1157	S[690]	1078	312.5
978	S[511]	3584	187.5	1038	S[571]	2744	187.5	1098	S[631]	1904	187.5	1158	S[691]	1064	187.5
979	S[512]	3570	312.5	1039	S[572]	2730	312.5	1099	S[632]	1890	312.5	1159	S[692]	1050	312.5
980	S[513]	3556	187.5	1040	S[573]	2716	187.5	1100	S[633]	1876	187.5	1160	S[693]	1036	187.5
981	S[514]	3542	312.5	1041	S[574]	2702	312.5	1101	S[634]	1862	312.5	1161	S[694]	1022	312.5
982	S[515]	3528	187.5	1042	S[575]	2688	187.5	1102	S[635]	1848	187.5	1162	S[695]	1008	187.5
983	S[516]	3514	312.5	1043	S[576]	2674	312.5	1103	S[636]	1834	312.5	1163	S[696]	994	312.5
984	S[517]	3500	187.5	1044	S[577]	2660	187.5	1104	S[637]	1820	187.5	1164	S[697]	980	187.5
985	S[518]	3486	312.5	1045	S[578]	2646	312.5	1105	S[638]	1806	312.5	1165	S[698]	966	312.5
986	S[519]	3472	187.5	1046	S[579]	2632	187.5	1106	S[639]	1792	187.5	1166	S[699]	952	187.5
987	S[520]	3458	312.5	1047	S[580]	2618	312.5	1107	S[640]	1778	312.5	1167	S[700]	938	312.5
988	S[521]	3444	187.5	1048	S[581]	2604	187.5	1108	S[641]	1764	187.5	1168	S[701]	924	187.5
989	S[522]	3430	312.5	1049	S[582]	2590	312.5	1109	S[642]	1750	312.5	1169	S[702]	910	312.5
990	S[523]	3416	187.5	1050	S[583]	2576	187.5	1110	S[643]	1736	187.5	1170	S[703]	896	187.5
991	S[524]	3402	312.5	1051	S[584]	2562	312.5	1111	S[644]	1722	312.5	1171	S[704]	882	312.5
992	S[525]	3388	187.5	1052	S[585]	2548	187.5	1112	S[645]	1708	187.5	1172	S[705]	868	187.5
993	S[526]	3374	312.5	1053	S[586]	2534	312.5	1113	S[646]	1694	312.5	1173	S[706]	854	312.5
994	S[527]	3360	187.5	1054	S[587]	2520	187.5	1114	S[647]	1680	187.5	1174	S[707]	840	187.5
995	S[528]	3346	312.5	1055	S[588]	2506	312.5	1115	S[648]	1666	312.5	1175	S[708]	826	312.5
996	S[529]	3332	187.5	1056	S[589]	2492	187.5	1116	S[649]	1652	187.5	1176	S[709]	812	187.5
997	S[530]	3318	312.5	1057	S[590]	2478	312.5	1117	S[650]	1638	312.5	1177	S[710]	798	312.5
998	S[531]	3304	187.5	1058	S[591]	2464	187.5	1118	S[651]	1624	187.5	1178	S[711]	784	187.5
999	S[532]	3290	312.5	1059	S[592]	2450	312.5	1119	S[652]	1610	312.5	1179	S[712]	770	312.5
1000	S[533]	3276	187.5	1060	S[593]	2436	187.5	1120	S[653]	1596	187.5	1180	S[713]	756	187.5
1001	S[534]	3262	312.5	1061	S[594]	2422	312.5	1121	S[654]	1582	312.5	1181	S[714]	742	312.5
1002	S[535]	3248	187.5	1062	S[595]	2408	187.5	1122	S[655]	1568	187.5	1182	S[715]	728	187.5
1003	S[536]	3234	312.5	1063	S[596]	2394	312.5	1123	S[656]	1554	312.5	1183	S[716]	714	312.5
1004	S[537]	3220	187.5	1064	S[597]	2380	187.5	1124	S[657]	1540	187.5	1184	S[717]	700	187.5
1005	S[538]	3206	312.5	1065	S[598]	2366	312.5	1125	S[658]	1526	312.5	1185	S[718]	686	312.5
1006	S[539]	3192	187.5	1066	S[599]	2352	187.5	1126	S[659]	1512	187.5	1186	S[719]	672	187.5
1007	S[540]	3178	312.5	1067	S[600]	2338	312.5	1127	S[660]	1498	312.5	1187	S[720]	658	312.5
1008	S[541]	3164	187.5	1068	S[601]	2324	187.5	1128	S[661]	1484	187.5	1188	DMY_VSS	644	187.5
1009	S[542]	3150	312.5	1069	S[602]	2310	312.5	1129	S[662]	1470	312.5	1189	DMY_VSS	630	312.5
1010	S[543]	3136	187.5	1070	S[603]	2296	187.5	1130	S[663]	1456	187.5	1190	DMY	616	187.5
1011	S[544]	3122	312.5	1071	S[604]	2282	312.5	1131	S[664]	1442	312.5	1191	DMY	602	312.5
1012	S[545]	3108	187.5	1072	S[605]	2268	187.5	1132	S[665]	1428	187.5	1192	DMY	588	187.5
1013	S[546]	3094	312.5	1073	S[606]	2254	312.5	1133	S[666]	1414	312.5	1193	DMY	574	312.5
1014	S[547]	3080	187.5	1074	S[607]	2240	187.5	1134	S[667]	1400	187.5	1194	DMY	560	187.5
1015	S[548]	3066	312.5	1075	S[608]	2226	312.5	1135	S[668]	1386	312.5	1195	DMY	546	312.5
1016	S[549]	3052	187.5	1076	S[609]	2212	187.5	1136	S[669]	1372	187.5	1196	DMY	532	187.5
1017	S[550]	3038	312.5	1077	S[610]	2198	312.5	1137	S[670]	1358	312.5	1197	DMY	518	312.5
1018	S[551]	3024	187.5	1078	S[611]	2184	187.5	1138	S[671]	1344	187.5	1198	DMY	504	187.5
1019	S[552]	3010	312.5	1079	S[612]	2170	312.5	1139	S[672]	1330	312.5	1199	DMY	490	312.5
1020	S[553]	2996	187.5	1080	S[613]	2156	187.5	1140	S[673]	1316	187.5	1200	DMY	476	187.5

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1201	DMY	462	312.5	1261	S[745]	-378	312.5	1321	S[805]	-1218	312.5	1381	S[865]	-2058	312.5
1202	DMY	448	187.5	1262	S[746]	-392	187.5	1322	S[806]	-1232	187.5	1382	S[866]	-2072	187.5
1203	DMY	434	312.5	1263	S[747]	-406	312.5	1323	S[807]	-1246	312.5	1383	S[867]	-2086	312.5
1204	DMY	420	187.5	1264	S[748]	-420	187.5	1324	S[808]	-1260	187.5	1384	S[868]	-2100	187.5
1205	DMY	406	312.5	1265	S[749]	-434	312.5	1325	S[809]	-1274	312.5	1385	S[869]	-2114	312.5
1206	DMY	392	187.5	1266	S[750]	-448	187.5	1326	S[810]	-1288	187.5	1386	S[870]	-2128	187.5
1207	DMY	378	312.5	1267	S[751]	-462	312.5	1327	S[811]	-1302	312.5	1387	S[871]	-2142	312.5
1208	DMY	364	187.5	1268	S[752]	-476	187.5	1328	S[812]	-1316	187.5	1388	S[872]	-2156	187.5
1209	DMY	350	312.5	1269	S[753]	-490	312.5	1329	S[813]	-1330	312.5	1389	S[873]	-2170	312.5
1210	DMY	336	187.5	1270	S[754]	-504	187.5	1330	S[814]	-1344	187.5	1390	S[874]	-2184	187.5
1211	DMY	322	312.5	1271	S[755]	-518	312.5	1331	S[815]	-1358	312.5	1391	S[875]	-2198	312.5
1212	DMY	308	187.5	1272	S[756]	-532	187.5	1332	S[816]	-1372	187.5	1392	S[876]	-2212	187.5
1213	DMY	294	312.5	1273	S[757]	-546	312.5	1333	S[817]	-1386	312.5	1393	S[877]	-2226	312.5
1214	DMY	280	187.5	1274	S[758]	-560	187.5	1334	S[818]	-1400	187.5	1394	S[878]	-2240	187.5
1215	DMY	266	312.5	1275	S[759]	-574	312.5	1335	S[819]	-1414	312.5	1395	S[879]	-2254	312.5
1216	DMY	252	187.5	1276	S[760]	-588	187.5	1336	S[820]	-1428	187.5	1396	S[880]	-2268	187.5
1217	DMY	238	312.5	1277	S[761]	-602	312.5	1337	S[821]	-1442	312.5	1397	S[881]	-2282	312.5
1218	DMY	224	187.5	1278	S[762]	-616	187.5	1338	S[822]	-1456	187.5	1398	S[882]	-2296	187.5
1219	DMY	210	312.5	1279	S[763]	-630	312.5	1339	S[823]	-1470	312.5	1399	S[883]	-2310	312.5
1220	DMY	196	187.5	1280	S[764]	-644	187.5	1340	S[824]	-1484	187.5	1400	S[884]	-2324	187.5
1221	DMY	182	312.5	1281	S[765]	-658	312.5	1341	S[825]	-1498	312.5	1401	S[885]	-2338	312.5
1222	DMY	168	187.5	1282	S[766]	-672	187.5	1342	S[826]	-1512	187.5	1402	S[886]	-2352	187.5
1223	DMY	154	312.5	1283	S[767]	-686	312.5	1343	S[827]	-1526	312.5	1403	S[887]	-2366	312.5
1224	DMY	140	187.5	1284	S[768]	-700	187.5	1344	S[828]	-1540	187.5	1404	S[888]	-2380	187.5
1225	DMY	126	312.5	1285	S[769]	-714	312.5	1345	S[829]	-1554	312.5	1405	S[889]	-2394	312.5
1226	DMY	112	187.5	1286	S[770]	-728	187.5	1346	S[830]	-1568	187.5	1406	S[890]	-2408	187.5
1227	DMY	98	312.5	1287	S[771]	-742	312.5	1347	S[831]	-1582	312.5	1407	S[891]	-2422	312.5
1228	DMY	84	187.5	1288	S[772]	-756	187.5	1348	S[832]	-1596	187.5	1408	S[892]	-2436	187.5
1229	DMY	70	312.5	1289	S[773]	-770	312.5	1349	S[833]	-1610	312.5	1409	S[893]	-2450	312.5
1230	DMY	56	187.5	1290	S[774]	-784	187.5	1350	S[834]	-1624	187.5	1410	S[894]	-2464	187.5
1231	DMY	42	312.5	1291	S[775]	-798	312.5	1351	S[835]	-1638	312.5	1411	S[895]	-2478	312.5
1232	DMY	28	187.5	1292	S[776]	-812	187.5	1352	S[836]	-1652	187.5	1412	S[896]	-2492	187.5
1233	DMY	14	312.5	1293	S[777]	-826	312.5	1353	S[837]	-1666	312.5	1413	S[897]	-2506	312.5
1234	DMY	0	187.5	1294	S[778]	-840	187.5	1354	S[838]	-1680	187.5	1414	S[898]	-2520	187.5
1235	DMY_VSS	-14	312.5	1295	S[779]	-854	312.5	1355	S[839]	-1694	312.5	1415	S[899]	-2534	312.5
1236	DMY_VSS	-28	187.5	1296	S[780]	-868	187.5	1356	S[840]	-1708	187.5	1416	S[900]	-2548	187.5
1237	S[721]	-42	312.5	1297	S[781]	-882	312.5	1357	S[841]	-1722	312.5	1417	S[901]	-2562	312.5
1238	S[722]	-56	187.5	1298	S[782]	-896	187.5	1358	S[842]	-1736	187.5	1418	S[902]	-2576	187.5
1239	S[723]	-70	312.5	1299	S[783]	-910	312.5	1359	S[843]	-1750	312.5	1419	S[903]	-2590	312.5
1240	S[724]	-84	187.5	1300	S[784]	-924	187.5	1360	S[844]	-1764	187.5	1420	S[904]	-2604	187.5
1241	S[725]	-98	312.5	1301	S[785]	-938	312.5	1361	S[845]	-1778	312.5	1421	S[905]	-2618	312.5
1242	S[726]	-112	187.5	1302	S[786]	-952	187.5	1362	S[846]	-1792	187.5	1422	S[906]	-2632	187.5
1243	S[727]	-126	312.5	1303	S[787]	-966	312.5	1363	S[847]	-1806	312.5	1423	S[907]	-2646	312.5
1244	S[728]	-140	187.5	1304	S[788]	-980	187.5	1364	S[848]	-1820	187.5	1424	S[908]	-2660	187.5
1245	S[729]	-154	312.5	1305	S[789]	-994	312.5	1365	S[849]	-1834	312.5	1425	S[909]	-2674	312.5
1246	S[730]	-168	187.5	1306	S[790]	-1008	187.5	1366	S[850]	-1848	187.5	1426	S[910]	-2688	187.5
1247	S[731]	-182	312.5	1307	S[791]	-1022	312.5	1367	S[851]	-1862	312.5	1427	S[911]	-2702	312.5
1248	S[732]	-196	187.5	1308	S[792]	-1036	187.5	1368	S[852]	-1876	187.5	1428	S[912]	-2716	187.5
1249	S[733]	-210	312.5	1309	S[793]	-1050	312.5	1369	S[853]	-1890	312.5	1429	S[913]	-2730	312.5
1250	S[734]	-224	187.5	1310	S[794]	-1064	187.5	1370	S[854]	-1904	187.5	1430	S[914]	-2744	187.5
1251	S[735]	-238	312.5	1311	S[795]	-1078	312.5	1371	S[855]	-1918	312.5	1431	S[915]	-2758	312.5
1252	S[736]	-252	187.5	1312	S[796]	-1092	187.5	1372	S[856]	-1932	187.5	1432	S[916]	-2772	187.5
1253	S[737]	-266	312.5	1313	S[797]	-1106	312.5	1373	S[857]	-1946	312.5	1433	S[917]	-2786	312.5
1254	S[738]	-280	187.5	1314	S[798]	-1120	187.5	1374	S[858]	-1960	187.5	1434	S[918]	-2800	187.5
1255	S[739]	-294	312.5	1315	S[799]	-1134	312.5	1375	S[859]	-1974	312.5	1435	S[919]	-2814	312.5
1256	S[740]	-308	187.5	1316	S[800]	-1148	187.5	1376	S[860]	-1988	187.5	1436	S[920]	-2828	187.5
1257	S[741]	-322	312.5	1317	S[801]	-1162	312.5	1377	S[861]	-2002	312.5	1437	S[921]	-2842	312.5
1258	S[742]	-336	187.5	1318	S[802]	-1176	187.5	1378	S[862]	-2016	187.5	1438	S[922]	-2856	187.5
1259	S[743]	-350	312.5	1319	S[803]	-1190	312.5	1379	S[863]	-2030	312.5	1439	S[923]	-2870	312.5
1260	S[744]	-364	187.5	1320	S[804]	-1204	187.5	1380	S[864]	-2044	187.5	1440	S[924]	-2884	187.5

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1441	S[925]	-2898	312.5	1501	S[985]	-3738	312.5	1561	S[1045]	-4578	312.5	1621	S[1105]	-5418	312.5
1442	S[926]	-2912	187.5	1502	S[986]	-3752	187.5	1562	S[1046]	-4592	187.5	1622	S[1106]	-5432	187.5
1443	S[927]	-2926	312.5	1503	S[987]	-3766	312.5	1563	S[1047]	-4606	312.5	1623	S[1107]	-5446	312.5
1444	S[928]	-2940	187.5	1504	S[988]	-3780	187.5	1564	S[1048]	-4620	187.5	1624	S[1108]	-5460	187.5
1445	S[929]	-2954	312.5	1505	S[989]	-3794	312.5	1565	S[1049]	-4634	312.5	1625	S[1109]	-5474	312.5
1446	S[930]	-2968	187.5	1506	S[990]	-3808	187.5	1566	S[1050]	-4648	187.5	1626	S[1110]	-5488	187.5
1447	S[931]	-2982	312.5	1507	S[991]	-3822	312.5	1567	S[1051]	-4662	312.5	1627	S[1111]	-5502	312.5
1448	S[932]	-2996	187.5	1508	S[992]	-3836	187.5	1568	S[1052]	-4676	187.5	1628	S[1112]	-5516	187.5
1449	S[933]	-3010	312.5	1509	S[993]	-3850	312.5	1569	S[1053]	-4690	312.5	1629	S[1113]	-5530	312.5
1450	S[934]	-3024	187.5	1510	S[994]	-3864	187.5	1570	S[1054]	-4704	187.5	1630	S[1114]	-5544	187.5
1451	S[935]	-3038	312.5	1511	S[995]	-3878	312.5	1571	S[1055]	-4718	312.5	1631	S[1115]	-5558	312.5
1452	S[936]	-3052	187.5	1512	S[996]	-3892	187.5	1572	S[1056]	-4732	187.5	1632	S[1116]	-5572	187.5
1453	S[937]	-3066	312.5	1513	S[997]	-3906	312.5	1573	S[1057]	-4746	312.5	1633	S[1117]	-5586	312.5
1454	S[938]	-3080	187.5	1514	S[998]	-3920	187.5	1574	S[1058]	-4760	187.5	1634	S[1118]	-5600	187.5
1455	S[939]	-3094	312.5	1515	S[999]	-3934	312.5	1575	S[1059]	-4774	312.5	1635	S[1119]	-5614	312.5
1456	S[940]	-3108	187.5	1516	S[1000]	-3948	187.5	1576	S[1060]	-4788	187.5	1636	S[1120]	-5628	187.5
1457	S[941]	-3122	312.5	1517	S[1001]	-3962	312.5	1577	S[1061]	-4802	312.5	1637	S[1121]	-5642	312.5
1458	S[942]	-3136	187.5	1518	S[1002]	-3976	187.5	1578	S[1062]	-4816	187.5	1638	S[1122]	-5656	187.5
1459	S[943]	-3150	312.5	1519	S[1003]	-3990	312.5	1579	S[1063]	-4830	312.5	1639	S[1123]	-5670	312.5
1460	S[944]	-3164	187.5	1520	S[1004]	-4004	187.5	1580	S[1064]	-4844	187.5	1640	S[1124]	-5684	187.5
1461	S[945]	-3178	312.5	1521	S[1005]	-4018	312.5	1581	S[1065]	-4858	312.5	1641	S[1125]	-5698	312.5
1462	S[946]	-3192	187.5	1522	S[1006]	-4032	187.5	1582	S[1066]	-4872	187.5	1642	S[1126]	-5712	187.5
1463	S[947]	-3206	312.5	1523	S[1007]	-4046	312.5	1583	S[1067]	-4886	312.5	1643	S[1127]	-5726	312.5
1464	S[948]	-3220	187.5	1524	S[1008]	-4060	187.5	1584	S[1068]	-4900	187.5	1644	S[1128]	-5740	187.5
1465	S[949]	-3234	312.5	1525	S[1009]	-4074	312.5	1585	S[1069]	-4914	312.5	1645	S[1129]	-5754	312.5
1466	S[950]	-3248	187.5	1526	S[1010]	-4088	187.5	1586	S[1070]	-4928	187.5	1646	S[1130]	-5768	187.5
1467	S[951]	-3262	312.5	1527	S[1011]	-4102	312.5	1587	S[1071]	-4942	312.5	1647	S[1131]	-5782	312.5
1468	S[952]	-3276	187.5	1528	S[1012]	-4116	187.5	1588	S[1072]	-4956	187.5	1648	S[1132]	-5796	187.5
1469	S[953]	-3290	312.5	1529	S[1013]	-4130	312.5	1589	S[1073]	-4970	312.5	1649	S[1133]	-5810	312.5
1470	S[954]	-3304	187.5	1530	S[1014]	-4144	187.5	1590	S[1074]	-4984	187.5	1650	S[1134]	-5824	187.5
1471	S[955]	-3318	312.5	1531	S[1015]	-4158	312.5	1591	S[1075]	-4998	312.5	1651	S[1135]	-5838	312.5
1472	S[956]	-3332	187.5	1532	S[1016]	-4172	187.5	1592	S[1076]	-5012	187.5	1652	S[1136]	-5852	187.5
1473	S[957]	-3346	312.5	1533	S[1017]	-4186	312.5	1593	S[1077]	-5026	312.5	1653	S[1137]	-5866	312.5
1474	S[958]	-3360	187.5	1534	S[1018]	-4200	187.5	1594	S[1078]	-5040	187.5	1654	S[1138]	-5880	187.5
1475	S[959]	-3374	312.5	1535	S[1019]	-4214	312.5	1595	S[1079]	-5054	312.5	1655	S[1139]	-5894	312.5
1476	S[960]	-3388	187.5	1536	S[1020]	-4228	187.5	1596	S[1080]	-5068	187.5	1656	S[1140]	-5908	187.5
1477	S[961]	-3402	312.5	1537	S[1021]	-4242	312.5	1597	S[1081]	-5082	312.5	1657	S[1141]	-5922	312.5
1478	S[962]	-3416	187.5	1538	S[1022]	-4256	187.5	1598	S[1082]	-5096	187.5	1658	S[1142]	-5936	187.5
1479	S[963]	-3430	312.5	1539	S[1023]	-4270	312.5	1599	S[1083]	-5110	312.5	1659	S[1143]	-5950	312.5
1480	S[964]	-3444	187.5	1540	S[1024]	-4284	187.5	1600	S[1084]	-5124	187.5	1660	S[1144]	-5964	187.5
1481	S[965]	-3458	312.5	1541	S[1025]	-4298	312.5	1601	S[1085]	-5138	312.5	1661	S[1145]	-5978	312.5
1482	S[966]	-3472	187.5	1542	S[1026]	-4312	187.5	1602	S[1086]	-5152	187.5	1662	S[1146]	-5992	187.5
1483	S[967]	-3486	312.5	1543	S[1027]	-4326	312.5	1603	S[1087]	-5166	312.5	1663	S[1147]	-6006	312.5
1484	S[968]	-3500	187.5	1544	S[1028]	-4340	187.5	1604	S[1088]	-5180	187.5	1664	S[1148]	-6020	187.5
1485	S[969]	-3514	312.5	1545	S[1029]	-4354	312.5	1605	S[1089]	-5194	312.5	1665	S[1149]	-6034	312.5
1486	S[970]	-3528	187.5	1546	S[1030]	-4368	187.5	1606	S[1090]	-5208	187.5	1666	S[1150]	-6048	187.5
1487	S[971]	-3542	312.5	1547	S[1031]	-4382	312.5	1607	S[1091]	-5222	312.5	1667	S[1151]	-6062	312.5
1488	S[972]	-3556	187.5	1548	S[1032]	-4396	187.5	1608	S[1092]	-5236	187.5	1668	S[1152]	-6076	187.5
1489	S[973]	-3570	312.5	1549	S[1033]	-4410	312.5	1609	S[1093]	-5250	312.5	1669	S[1153]	-6090	312.5
1490	S[974]	-3584	187.5	1550	S[1034]	-4424	187.5	1610	S[1094]	-5264	187.5	1670	S[1154]	-6104	187.5
1491	S[975]	-3598	312.5	1551	S[1035]	-4438	312.5	1611	S[1095]	-5278	312.5	1671	S[1155]	-6118	312.5
1492	S[976]	-3612	187.5	1552	S[1036]	-4452	187.5	1612	S[1096]	-5292	187.5	1672	S[1156]	-6132	187.5
1493	S[977]	-3626	312.5	1553	S[1037]	-4466	312.5	1613	S[1097]	-5306	312.5	1673	S[1157]	-6146	312.5
1494	S[978]	-3640	187.5	1554	S[1038]	-4480	187.5	1614	S[1098]	-5320	187.5	1674	S[1158]	-6160	187.5
1495	S[979]	-3654	312.5	1555	S[1039]	-4494	312.5	1615	S[1099]	-5334	312.5	1675	S[1159]	-6174	312.5
1496	S[980]	-3668	187.5	1556	S[1040]	-4508	187.5	1616	S[1100]	-5348	187.5	1676	S[1160]	-6188	187.5
1497	S[981]	-3682	312.5	1557	S[1041]	-4522	312.5	1617	S[1101]	-5362	312.5	1677	S[1161]	-6202	312.5
1498	S[982]	-3696	187.5	1558	S[1042]	-4536	187.5	1618	S[1102]	-5376	187.5	1678	S[1162]	-6216	187.5
1499	S[983]	-3710	312.5	1559	S[1043]	-4550	312.5	1619	S[1103]	-5390	312.5	1679	S[1163]	-6230	312.5
1500	S[984]	-3724	187.5	1560	S[1044]	-4564	187.5	1620	S[1104]	-5404	187.5	1680	S[1164]	-6244	187.5

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1681	S[1165]	-6258	312.5	1741	S[1225]	-7098	312.5	1801	S[1285]	-7938	312.5	1861	S[1345]	-8778	312.5
1682	S[1166]	-6272	187.5	1742	S[1226]	-7112	187.5	1802	S[1286]	-7952	187.5	1862	S[1346]	-8792	187.5
1683	S[1167]	-6286	312.5	1743	S[1227]	-7126	312.5	1803	S[1287]	-7966	312.5	1863	S[1347]	-8806	312.5
1684	S[1168]	-6300	187.5	1744	S[1228]	-7140	187.5	1804	S[1288]	-7980	187.5	1864	S[1348]	-8820	187.5
1685	S[1169]	-6314	312.5	1745	S[1229]	-7154	312.5	1805	S[1289]	-7994	312.5	1865	S[1349]	-8834	312.5
1686	S[1170]	-6328	187.5	1746	S[1230]	-7168	187.5	1806	S[1290]	-8008	187.5	1866	S[1350]	-8848	187.5
1687	S[1171]	-6342	312.5	1747	S[1231]	-7182	312.5	1807	S[1291]	-8022	312.5	1867	S[1351]	-8862	312.5
1688	S[1172]	-6356	187.5	1748	S[1232]	-7196	187.5	1808	S[1292]	-8036	187.5	1868	S[1352]	-8876	187.5
1689	S[1173]	-6370	312.5	1749	S[1233]	-7210	312.5	1809	S[1293]	-8050	312.5	1869	S[1353]	-8890	312.5
1690	S[1174]	-6384	187.5	1750	S[1234]	-7224	187.5	1810	S[1294]	-8064	187.5	1870	S[1354]	-8904	187.5
1691	S[1175]	-6398	312.5	1751	S[1235]	-7238	312.5	1811	S[1295]	-8078	312.5	1871	S[1355]	-8918	312.5
1692	S[1176]	-6412	187.5	1752	S[1236]	-7252	187.5	1812	S[1296]	-8092	187.5	1872	S[1356]	-8932	187.5
1693	S[1177]	-6426	312.5	1753	S[1237]	-7266	312.5	1813	S[1297]	-8106	312.5	1873	S[1357]	-8946	312.5
1694	S[1178]	-6440	187.5	1754	S[1238]	-7280	187.5	1814	S[1298]	-8120	187.5	1874	S[1358]	-8960	187.5
1695	S[1179]	-6454	312.5	1755	S[1239]	-7294	312.5	1815	S[1299]	-8134	312.5	1875	S[1359]	-8974	312.5
1696	S[1180]	-6468	187.5	1756	S[1240]	-7308	187.5	1816	S[1300]	-8148	187.5	1876	S[1360]	-8988	187.5
1697	S[1181]	-6482	312.5	1757	S[1241]	-7322	312.5	1817	S[1301]	-8162	312.5	1877	S[1361]	-9002	312.5
1698	S[1182]	-6496	187.5	1758	S[1242]	-7336	187.5	1818	S[1302]	-8176	187.5	1878	S[1362]	-9016	187.5
1699	S[1183]	-6510	312.5	1759	S[1243]	-7350	312.5	1819	S[1303]	-8190	312.5	1879	S[1363]	-9030	312.5
1700	S[1184]	-6524	187.5	1760	S[1244]	-7364	187.5	1820	S[1304]	-8204	187.5	1880	S[1364]	-9044	187.5
1701	S[1185]	-6538	312.5	1761	S[1245]	-7378	312.5	1821	S[1305]	-8218	312.5	1881	S[1365]	-9058	312.5
1702	S[1186]	-6552	187.5	1762	S[1246]	-7392	187.5	1822	S[1306]	-8232	187.5	1882	S[1366]	-9072	187.5
1703	S[1187]	-6566	312.5	1763	S[1247]	-7406	312.5	1823	S[1307]	-8246	312.5	1883	S[1367]	-9086	312.5
1704	S[1188]	-6580	187.5	1764	S[1248]	-7420	187.5	1824	S[1308]	-8260	187.5	1884	S[1368]	-9100	187.5
1705	S[1189]	-6594	312.5	1765	S[1249]	-7434	312.5	1825	S[1309]	-8274	312.5	1885	S[1369]	-9114	312.5
1706	S[1190]	-6608	187.5	1766	S[1250]	-7448	187.5	1826	S[1310]	-8288	187.5	1886	S[1370]	-9128	187.5
1707	S[1191]	-6622	312.5	1767	S[1251]	-7462	312.5	1827	S[1311]	-8302	312.5	1887	S[1371]	-9142	312.5
1708	S[1192]	-6636	187.5	1768	S[1252]	-7476	187.5	1828	S[1312]	-8316	187.5	1888	S[1372]	-9156	187.5
1709	S[1193]	-6650	312.5	1769	S[1253]	-7490	312.5	1829	S[1313]	-8330	312.5	1889	S[1373]	-9170	312.5
1710	S[1194]	-6664	187.5	1770	S[1254]	-7504	187.5	1830	S[1314]	-8344	187.5	1890	S[1374]	-9184	187.5
1711	S[1195]	-6678	312.5	1771	S[1255]	-7518	312.5	1831	S[1315]	-8358	312.5	1891	S[1375]	-9198	312.5
1712	S[1196]	-6692	187.5	1772	S[1256]	-7532	187.5	1832	S[1316]	-8372	187.5	1892	S[1376]	-9212	187.5
1713	S[1197]	-6706	312.5	1773	S[1257]	-7546	312.5	1833	S[1317]	-8386	312.5	1893	S[1377]	-9226	312.5
1714	S[1198]	-6720	187.5	1774	S[1258]	-7560	187.5	1834	S[1318]	-8400	187.5	1894	S[1378]	-9240	187.5
1715	S[1199]	-6734	312.5	1775	S[1259]	-7574	312.5	1835	S[1319]	-8414	312.5	1895	S[1379]	-9254	312.5
1716	S[1200]	-6748	187.5	1776	S[1260]	-7588	187.5	1836	S[1320]	-8428	187.5	1896	S[1380]	-9268	187.5
1717	S[1201]	-6762	312.5	1777	S[1261]	-7602	312.5	1837	S[1321]	-8442	312.5	1897	S[1381]	-9282	312.5
1718	S[1202]	-6776	187.5	1778	S[1262]	-7616	187.5	1838	S[1322]	-8456	187.5	1898	S[1382]	-9296	187.5
1719	S[1203]	-6790	312.5	1779	S[1263]	-7630	312.5	1839	S[1323]	-8470	312.5	1899	S[1383]	-9310	312.5
1720	S[1204]	-6804	187.5	1780	S[1264]	-7644	187.5	1840	S[1324]	-8484	187.5	1900	S[1384]	-9324	187.5
1721	S[1205]	-6818	312.5	1781	S[1265]	-7658	312.5	1841	S[1325]	-8498	312.5	1901	S[1385]	-9338	312.5
1722	S[1206]	-6832	187.5	1782	S[1266]	-7672	187.5	1842	S[1326]	-8512	187.5	1902	S[1386]	-9352	187.5
1723	S[1207]	-6846	312.5	1783	S[1267]	-7686	312.5	1843	S[1327]	-8526	312.5	1903	S[1387]	-9366	312.5
1724	S[1208]	-6860	187.5	1784	S[1268]	-7700	187.5	1844	S[1328]	-8540	187.5	1904	S[1388]	-9380	187.5
1725	S[1209]	-6874	312.5	1785	S[1269]	-7714	312.5	1845	S[1329]	-8554	312.5	1905	S[1389]	-9394	312.5
1726	S[1210]	-6888	187.5	1786	S[1270]	-7728	187.5	1846	S[1330]	-8568	187.5	1906	S[1390]	-9408	187.5
1727	S[1211]	-6902	312.5	1787	S[1271]	-7742	312.5	1847	S[1331]	-8582	312.5	1907	S[1391]	-9422	312.5
1728	S[1212]	-6916	187.5	1788	S[1272]	-7756	187.5	1848	S[1332]	-8596	187.5	1908	S[1392]	-9436	187.5
1729	S[1213]	-6930	312.5	1789	S[1273]	-7770	312.5	1849	S[1333]	-8610	312.5	1909	S[1393]	-9450	312.5
1730	S[1214]	-6944	187.5	1790	S[1274]	-7784	187.5	1850	S[1334]	-8624	187.5	1910	S[1394]	-9464	187.5
1731	S[1215]	-6958	312.5	1791	S[1275]	-7798	312.5	1851	S[1335]	-8638	312.5	1911	S[1395]	-9478	312.5
1732	S[1216]	-6972	187.5	1792	S[1276]	-7812	187.5	1852	S[1336]	-8652	187.5	1912	S[1396]	-9492	187.5
1733	S[1217]	-6986	312.5	1793	S[1277]	-7826	312.5	1853	S[1337]	-8666	312.5	1913	S[1397]	-9506	312.5
1734	S[1218]	-7000	187.5	1794	S[1278]	-7840	187.5	1854	S[1338]	-8680	187.5	1914	S[1398]	-9520	187.5
1735	S[1219]	-7014	312.5	1795	S[1279]	-7854	312.5	1855	S[1339]	-8694	312.5	1915	S[1399]	-9534	312.5
1736	S[1220]	-7028	187.5	1796	S[1280]	-7868	187.5	1856	S[1340]	-8708	187.5	1916	S[1400]	-9548	187.5
1737	S[1221]	-7042	312.5	1797	S[1281]	-7882	312.5	1857	S[1341]	-8722	312.5	1917	S[1401]	-9562	312.5
1738	S[1222]	-7056	187.5	1798	S[1282]	-7896	187.5	1858	S[1342]	-8736	187.5	1918	S[1402]	-9576	187.5
1739	S[1223]	-7070	312.5	1799	S[1283]	-7910	312.5	1859	S[1343]	-8750	312.5	1919	S[1403]	-9590	312.5
1740	S[1224]	-7084	187.5	1800	S[1284]	-7924	187.5	1860	S[1344]	-8764	187.5	1920	S[1404]	-9604	187.5

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No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	Pad Name	X	Y
1921	S[1405]	-9618	312.5	1981	DMY	-10514	312.5	2041	GOUT[28]	-11354	312.5	ALMARK_R_T	11870	305
1922	S[1406]	-9632	187.5	1982	DMY	-10528	187.5	2042	GOUT[29]	-11368	187.5	ALMARK_L_T	-11870	305
1923	S[1407]	-9646	312.5	1983	DMY	-10542	312.5	2043	GOUT[29]	-11382	312.5			
1924	S[1408]	-9660	187.5	1984	DMY	-10556	187.5	2044	GOUT[30]	-11396	187.5			
1925	S[1409]	-9674	312.5	1985	DMY	-10570	312.5	2045	GOUT[30]	-11410	312.5			
1926	S[1410]	-9688	187.5	1986	DMY	-10584	187.5	2046	GOUT_VGLO	-11424	187.5			
1927	S[1411]	-9702	312.5	1987	DMY	-10598	312.5	2047	GOUT_VGLO	-11438	312.5			
1928	S[1412]	-9716	187.5	1988	DMY	-10612	187.5	2048	GOUT_VGLO	-11452	187.5			
1929	S[1413]	-9730	312.5	1989	DMY	-10626	312.5	2049	VGH_REG	-11466	312.5			
1930	S[1414]	-9744	187.5	1990	DMY	-10640	187.5	2050	VGH_REG	-11480	187.5			
1931	S[1415]	-9758	312.5	1991	DMY	-10654	312.5	2051	VGH_REG	-11494	312.5			
1932	S[1416]	-9772	187.5	1992	DMY	-10668	187.5	2052	LVGL	-11508	187.5			
1933	S[1417]	-9786	312.5	1993	DMY	-10682	312.5	2053	LVGL	-11522	312.5			
1934	S[1418]	-9800	187.5	1994	DMY	-10696	187.5	2054	LVGL	-11536	187.5			
1935	S[1419]	-9814	312.5	1995	DMY	-10710	312.5	2055	GOUT[31]	-11550	312.5			
1936	S[1420]	-9828	187.5	1996	DMY	-10724	187.5	2056	GOUT[31]	-11564	187.5			
1937	S[1421]	-9842	312.5	1997	DMY	-10738	312.5	2057	GOUT[32]	-11578	312.5			
1938	S[1422]	-9856	187.5	1998	DMY	-10752	187.5	2058	GOUT[32]	-11592	187.5			
1939	S[1423]	-9870	312.5	1999	DMY	-10766	312.5	2059	GOUT_VGLO	-11606	312.5			
1940	S[1424]	-9884	187.5	2000	DMY	-10780	187.5	2060	GOUT_VGLO	-11620	187.5			
1941	S[1425]	-9898	312.5	2001	DMY	-10794	312.5	2061	GOUT_VGLO	-11634	312.5			
1942	S[1426]	-9912	187.5	2002	DMY	-10808	187.5	2062	GOUT_VGHO	-11648	187.5			
1943	S[1427]	-9926	312.5	2003	DMY	-10822	312.5	2063	GOUT_VGHO	-11662	312.5			
1944	S[1428]	-9940	187.5	2004	DMY	-10836	187.5	2064	GOUT_VGHO	-11676	187.5			
1945	S[1429]	-9954	312.5	2005	DMY	-10850	312.5	2065	PADA4	-11690	312.5			
1946	S[1430]	-9968	187.5	2006	DMY	-10864	187.5	2066	PADB4	-11704	187.5			
1947	S[1431]	-9982	312.5	2007	DMY	-10878	312.5	2067	DMY_VSS	-11718	312.5			
1948	S[1432]	-9996	187.5	2008	DMY	-10892	187.5	2068	DMY_VSS	-11732	187.5			
1949	S[1433]	-10010	312.5	2009	DMY	-10906	312.5	2069	DMY_VSS	-11760	312.5			
1950	S[1434]	-10024	187.5	2010	DMY	-10920	187.5							
1951	S[1435]	-10038	312.5	2011	DMY	-10934	312.5							
1952	S[1436]	-10052	187.5	2012	DMY	-10948	187.5							
1953	S[1437]	-10066	312.5	2013	DMY	-10962	312.5							
1954	S[1438]	-10080	187.5	2014	DMY	-10976	187.5							
1955	S[1439]	-10094	312.5	2015	DMY	-10990	312.5							
1956	S[1440]	-10108	187.5	2016	DMY_VSS	-11004	187.5							
1957	S[1441]	-10122	312.5	2017	DMY_VSS	-11018	312.5							
1958	DMY_VSS	-10136	187.5	2018	GOUT[17]	-11032	187.5							
1959	DMY_VSS	-10150	312.5	2019	GOUT[17]	-11046	312.5							
1960	GOUT_VGLO	-10220	187.5	2020	GOUT[18]	-11060	187.5							
1961	GOUT_VGLO	-10234	312.5	2021	GOUT[18]	-11074	312.5							
1962	GOUT_VGLO	-10248	187.5	2022	GOUT[19]	-11088	187.5							
1963	GOUT_VGLO	-10262	312.5	2023	GOUT[19]	-11102	312.5							
1964	GOUT_VGLO	-10276	187.5	2024	GOUT[20]	-11116	187.5							
1965	GOUT_VGLO	-10290	312.5	2025	GOUT[20]	-11130	312.5							
1966	DMY_VGH	-10304	187.5	2026	GOUT[21]	-11144	187.5							
1967	DMY_VGH	-10318	312.5	2027	GOUT[21]	-11158	312.5							
1968	GOUT_VGHO	-10332	187.5	2028	GOUT[22]	-11172	187.5							
1969	GOUT_VGHO	-10346	312.5	2029	GOUT[22]	-11186	312.5							
1970	GOUT_VGHO	-10360	187.5	2030	GOUT[23]	-11200	187.5							
1971	GOUT_VGHO	-10374	312.5	2031	GOUT[23]	-11214	312.5							
1972	GOUT_VGHO	-10388	187.5	2032	GOUT[24]	-11228	187.5							
1973	GOUT_VGHO	-10402	312.5	2033	GOUT[24]	-11242	312.5							
1974	DMY_VSS	-10416	187.5	2034	GOUT[25]	-11256	187.5							
1975	DMY_VSS	-10430	312.5	2035	GOUT[25]	-11270	312.5							
1976	DMY	-10444	187.5	2036	GOUT[26]	-11284	187.5							
1977	DMY	-10458	312.5	2037	GOUT[26]	-11298	312.5							
1978	DMY	-10472	187.5	2038	GOUT[27]	-11312	187.5							
1979	DMY	-10486	312.5	2039	GOUT[27]	-11326	312.5							
1980	DMY	-10500	187.5	2040	GOUT[28]	-11340	187.5							

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3. System Interface

3.1. SPI Interface

The following is selection of interface decided by the IM [3:0] pins. See Table 8.

Table 8 SPI Interface

IM3	IM2	IM1	IM0	SPI Mode	CSX	SCL	Function
0	0	1	1	3-line serial interface	"L"	↑	Read/Write command, parameter.
1	0	0	1		"L"	↑	
1	0	1	0		"L"	↑	
1	0	1	1		"L"	↓	

The ILI9806E-2C uses a 3-line 9-bit serial interface for communication between the host and the ILI9806E-2C. The 3-line serial interface consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). If the data bus (DB [23:0]) is not used for the data transfer of DPI interface, the unused pins are unaffected. The Serial clock (SCL) is used only for the interface with the MPU, so it can be stopped when no communication is necessary.

3.1.1. Write Cycle Sequence

In write mode of the interface, the host writes commands and data to the ILI9806E-2C. The 3-line serial data packet contains a D/C (data/command) select bit and a transmission byte. If the D/C bit is "low", the transmission byte is interpreted as a command byte. If the D/C bit is "high", the transmission byte is stored in the command register as a parameter data.

Any instruction can be sent in any order to the ILI9806E-2C and the MSB is transmitted first. The serial interface is initialized when the CSX status is high. In this state, SCL clock pulse and SDI data are ineffective. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detail of data format for 3-line serial interface.

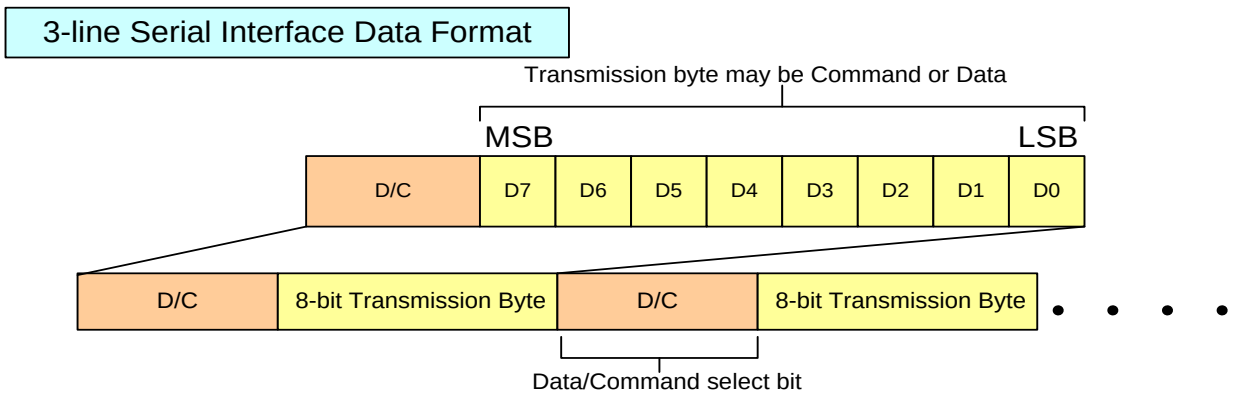


Figure 2 DBI data format

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The host drives the CSX pin to low and setting the D/C bit on the SDI pin. The bit is read by the ILI9806E-2C on the first rising edge of the SCL signal. On the next falling edge of the SCL, the MSB data bit (D7) is set on the SDI pin by the host. On the next falling edge of the SCL, the next bit (D6) is set on the SDI pin. If the optional D/C signal is used, a byte is eight read cycles long. The 3-line serial interface writes sequences described in the Figure 3 below.

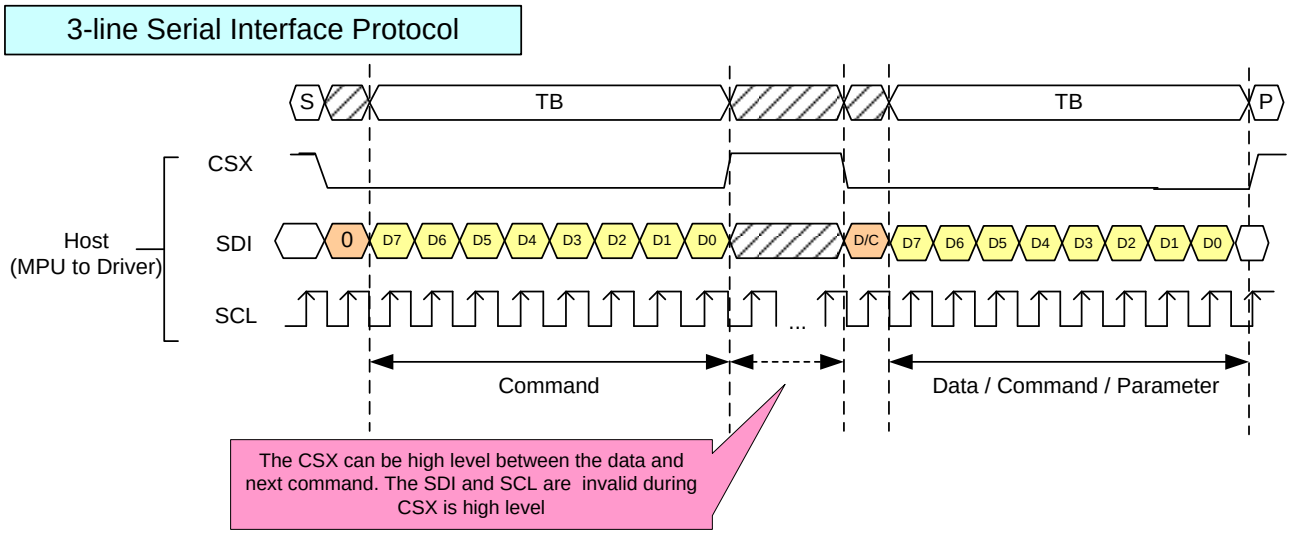


Figure 3 SPI protocol (SCL rising edge example)

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3.1.2. Read Cycle Sequence

In read mode of the interface, the host reads the register value from the ILI9806E-2C. The host sends a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The ILI9806E-2C samples the SDI (input data) at the rising edges of the SCL (serial clock), and shifts SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)

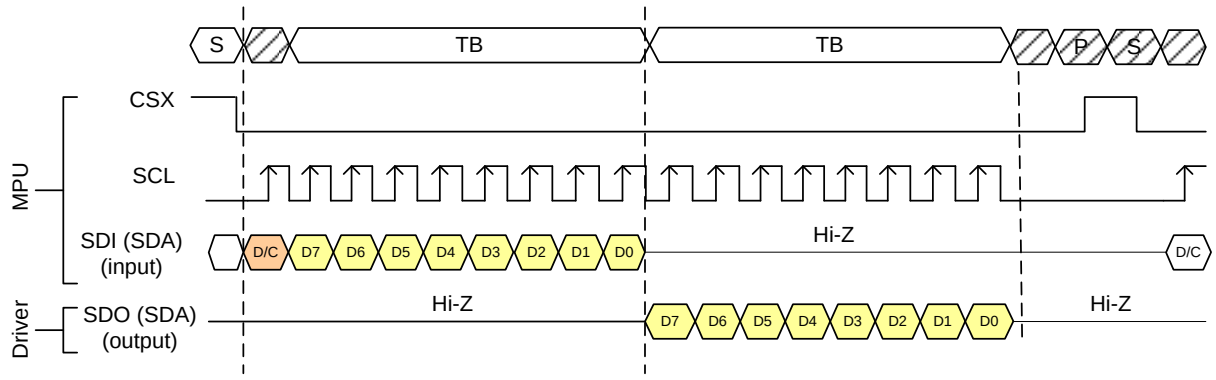


Figure 4 SPI read cycle sequence (SCL rising edge example)

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3.2. Data Transfer Break and Recovery

If there data transmission is broken by CSX pulse while transferring a Command, Multiple parameter command, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and reset the interface so it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

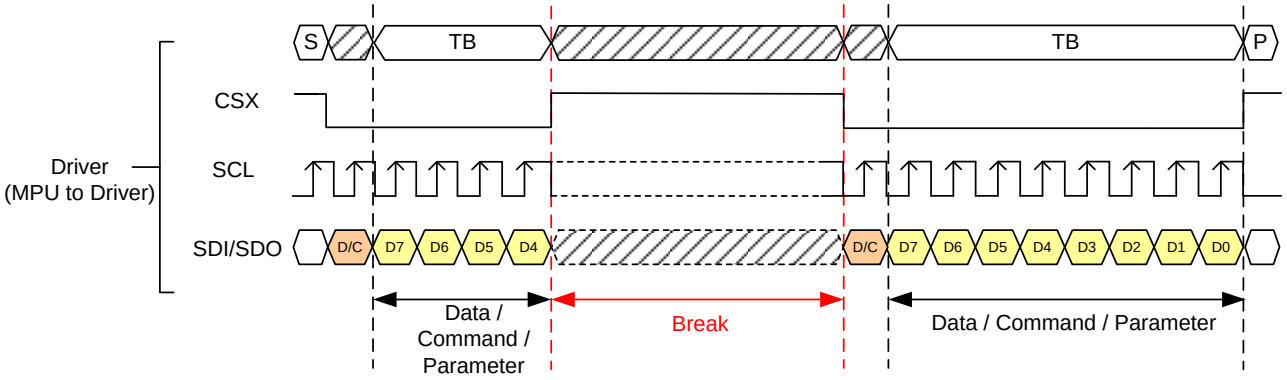


Figure 5 Data Transfer Break and Recovery (SCL rising edge example)

If there is a break in data transmission of a multiple parameter command, and the host initiates transfer of a new command, the parameters that were successfully transferred are stored and the incomplete parameter data where the break occurred is dropped. The interface is ready to receive the next byte as shown in the figure below. See diagram

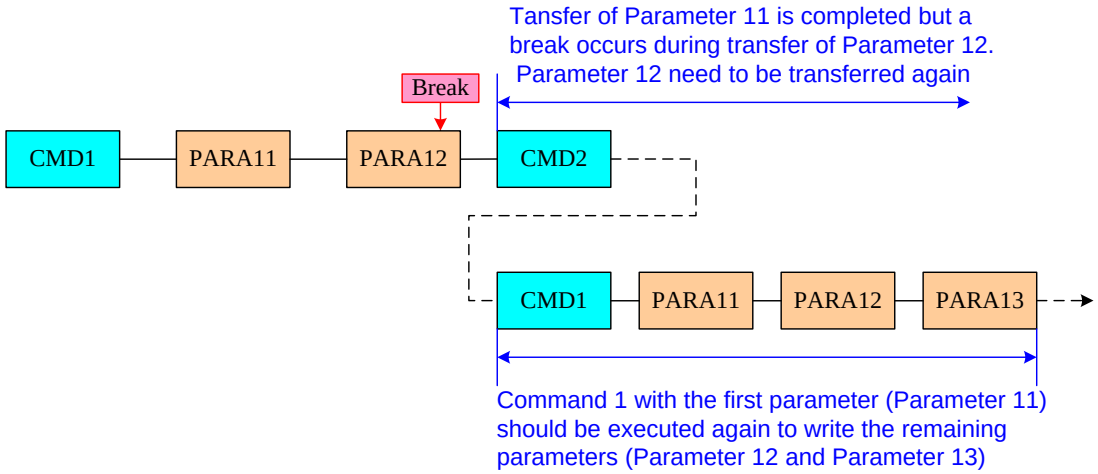


Figure 6 Data Transfer Break -Case 1

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If a multiple parameter command is sent and a break occurs when a new command is sent before all the parameters are transferred, then the parameters that were successfully sent are stored and the remaining parameters of that command remain at the previous value.

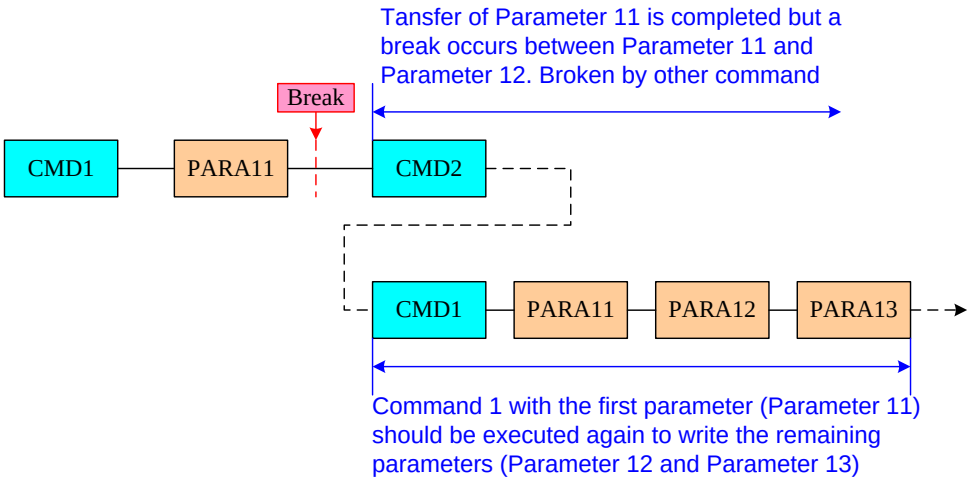


Figure 7 Data Transfer Break -Case 2

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3.3. Data Transfer Pause

It will be possible when transferring a Command, Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select pin (CSX) is released after Multiple Parameter Data has been completed, then the ILI9806E-2C will wait and continue Parameter Data Transmission from the point where it was paused. If the Chip Select pin is released after a whole byte of a command has been completely transmitted, then the display module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below.

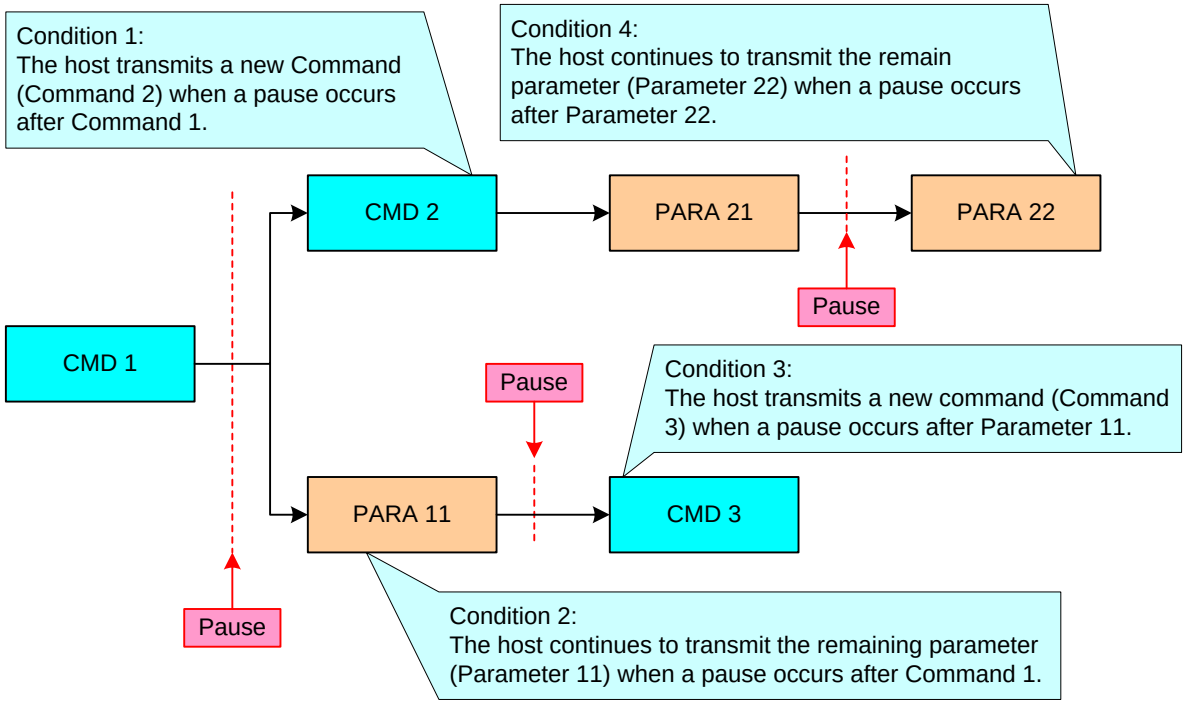


Figure 8 Data Transfer Pause

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3.3.1. Serial Interface Pause

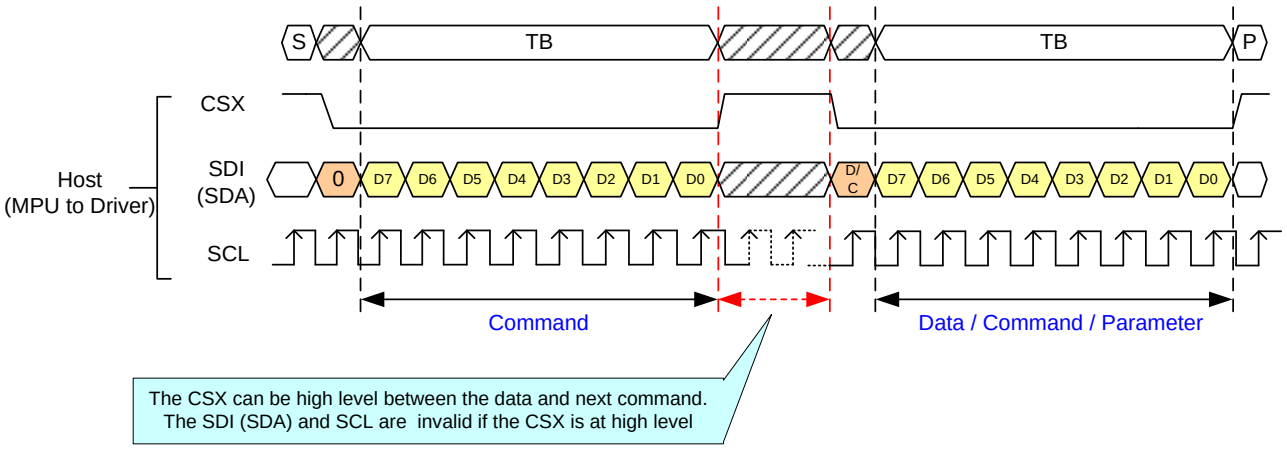


Figure 9 SPI data transfer pause (SCL rising edge example)

This applies to the following 4 conditions:

1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

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3.4. DPI (RGB) Interface

The DPI interface displaying moving pictures is selected by the ILI9806E-2C.

3.4.1. DPI Interface Selection

The DPI interface is operated with VS, HS, DE PCLK, DB [23:0] lines. It supports several pixel formats that can be selected by DPI [2:0] bits in “Pixel Format Set (R3Ah)” of Page 0 command. The selection of a given interface is defined by DPI [2:0] as show in the Table 9 and Figure 10 below.

Table 9 DPI (RGB) Interface Selection

DPI [2:0]			DPI (RGB) Interface Mode	Used Pins
1	0	1	16-bit RGB interface	VS, HS, DE, PCLK,DB [20:16] , DB [13:8], DB [4:0]
1	1	0	18-bit RGB interface	VS, HS, DE, PCLK, DB [21:16] , DB [13:8], DB [5:0]
1	1	1	24-bit RGB interface	VS, HS, DE, PCLK, DB [23:0]
Others			Setting prohibited	

16-bit DPI interface connection:set pixel format DPI[2:0]=3'h5

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]				B[4]	B[3]	B[2]	B[1]	B[0]

18-bit DPI interface connection:set pixel format DPI[2:0]=3'h6

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		R[5]	R4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

24-bit DPI interface connection:set pixel format DPI[2:0]=3'h7

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R[7]	R[6]	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Figure 10 DPI (RGB) Interface 16/18/24-bit pixel format selection

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The Pixel clock (PCLK) is running all the time without stopping, it is used for entering VS, HS, DE and DB [23:0] states when there is a rising edge of the PCLK. The PCLK can not be used as the internal clock for other functions of the display module.

Vertical synchronization (Vsync) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. DB [23:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of PCLK). DB [23:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the PCLK signal.

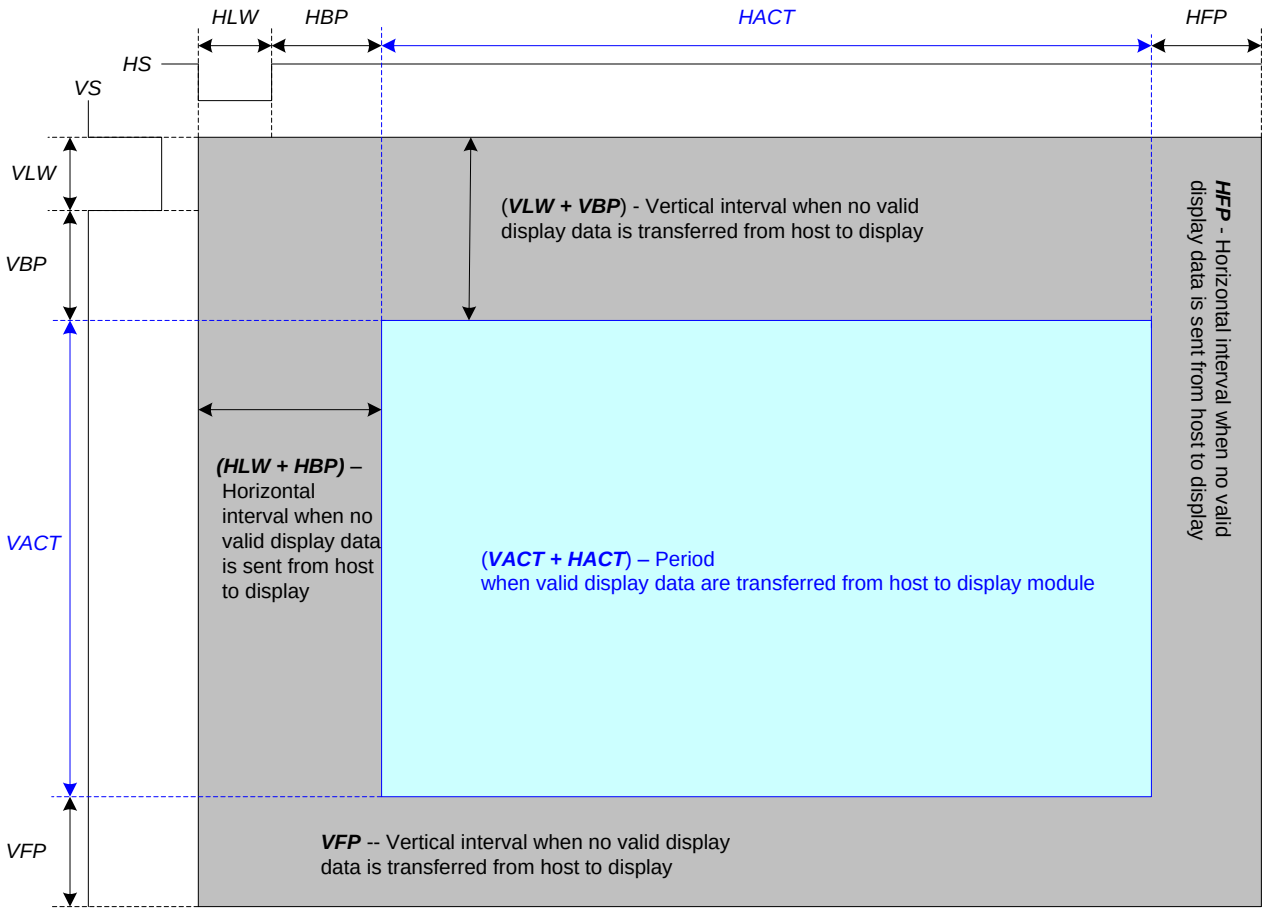
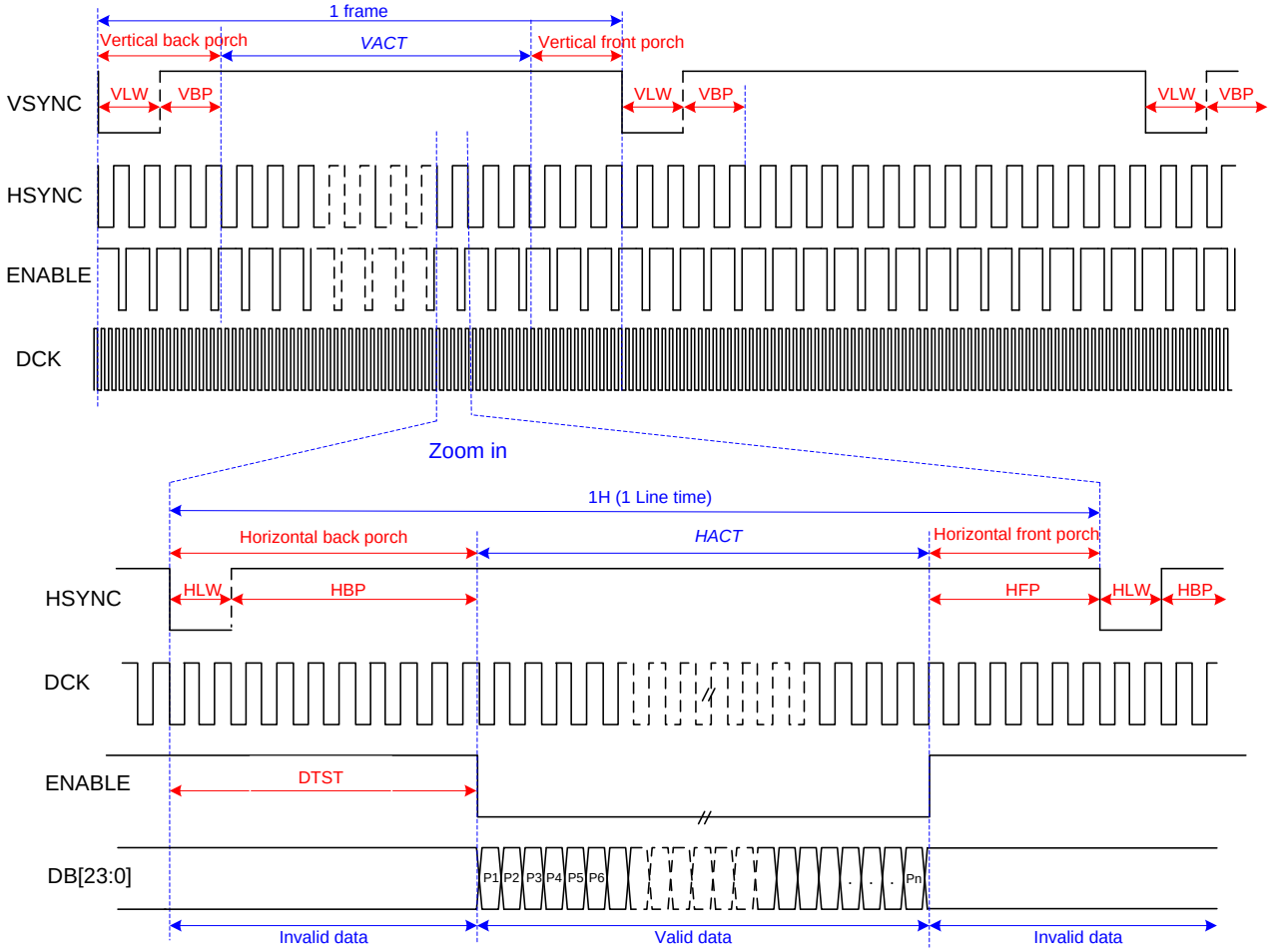


Figure 11 General DPI timing diagram

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3.4.2. DPI Interface Timing

The timing chart of 24-/18-/16-bit DPI (RGB) interface mode is illustrated in Figure 12.



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2…, pixel n.

Parameter	Symbols	Condition	Min.	Typ.	Max.	Units
Frame Rate	FR		54		66	fps
Horizontal Low Pulse width	HLW		1		-	DOTCLK
Horizontal Back Porch	HBP		2		126	DOTCLK
Horizontal Address	HACT			480		DOTCLK
Horizontal Front Porch	HFP		2		-	DOTCLK
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.6		35.7	MHz

Figure 12 DPI Interface Timing diagram[Note1,Note2]

Note1. HLW+HBP+HFP >= 4.5us.
Note2. VSPL='0', HSPL='0', DPL='0' and EPL='0' of "(Interface Mode Control 21h of the Page 1)" command.

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3.5. DSI system interface

3.5.1. General Description

The MIPI DSI is enabled or disabled by external IM[3:0] pin.

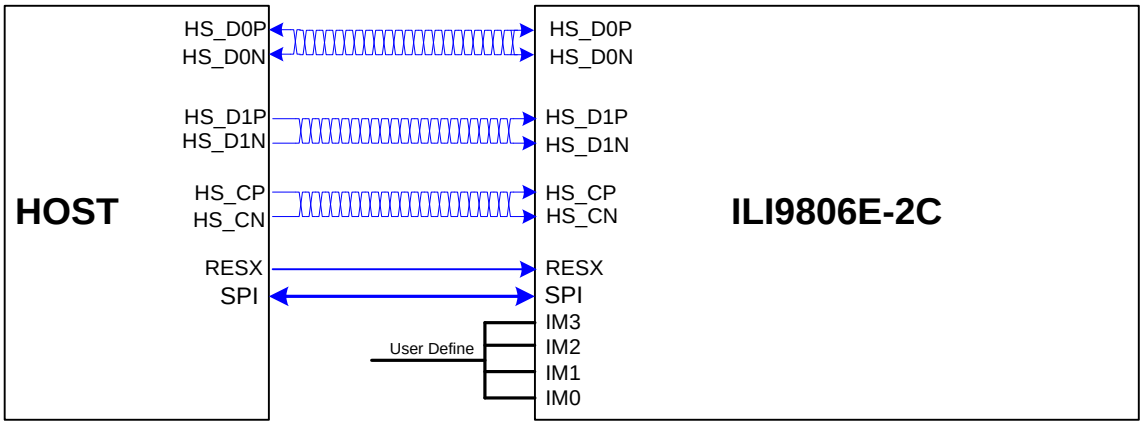


Figure 13 DSI system interface diagram

IM3	IM2	IM1	IM0	MPU Interface	Data Pin in Use
0	1	0	1	DSI interface	HS_CP, HS_CN HS_D0P, HS_D0N HS_D1P, HS_D1N
0	1	1	1	DSI+SPI interface	HS_CP, HS_CN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, SDI,SDO, SCL(rising edge), CSX
1	1	1	1	DSI+SPI interface	HS_CP, HS_CN, HS_D0P, HS_D0N, HS_D1P, HS_D1N, SDI,SDO, SCL(falling edge), CSX

The communication is separated into two different levels between the MPU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

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3.5.2. Interface Level Communication

3.5.3. General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MPU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 10 High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Note 1 *Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.*

Note 2 *If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.*

Note 3 *n = 0 and 1 (D1+/- lanes only for HS-0 and HS-1)*

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3.5.4. DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

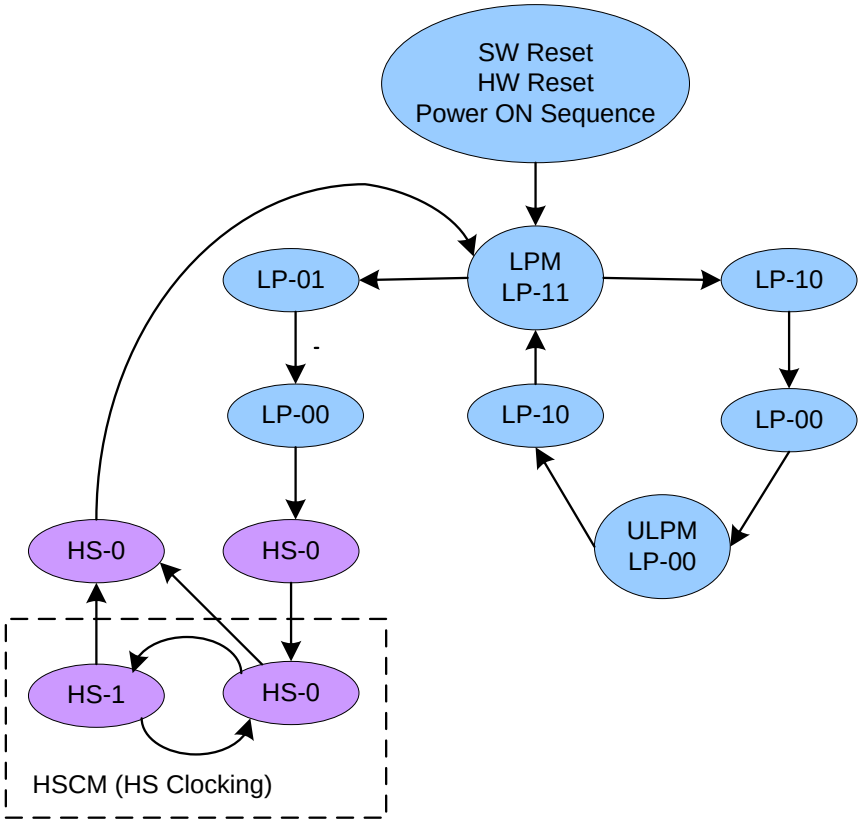


Figure 14 Clock Lanes Power Modes

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3.5.5. Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM).

This sequence is illustrated below.

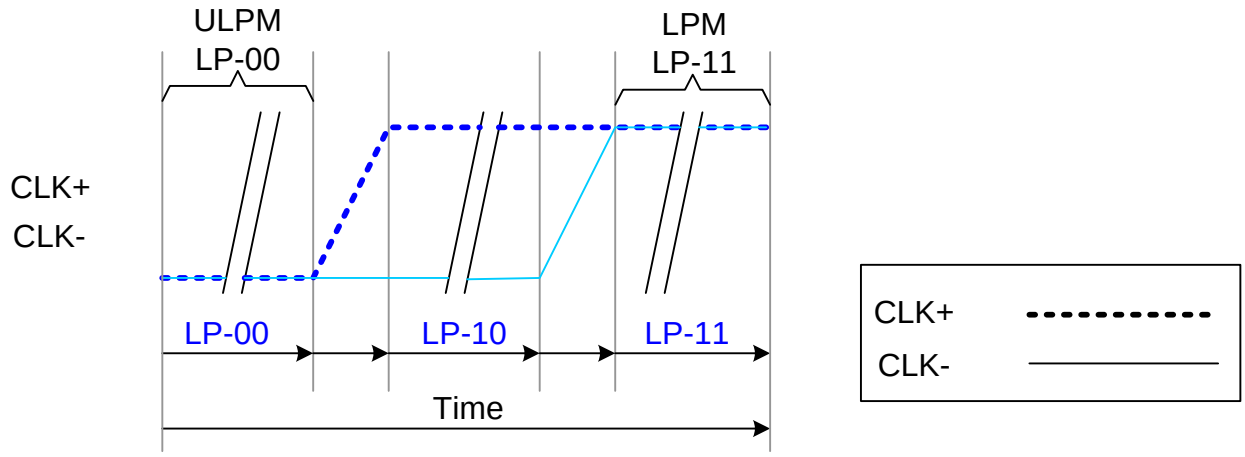


Figure 15 From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0=>LP-11 (LPM). This sequence is illustrated below.

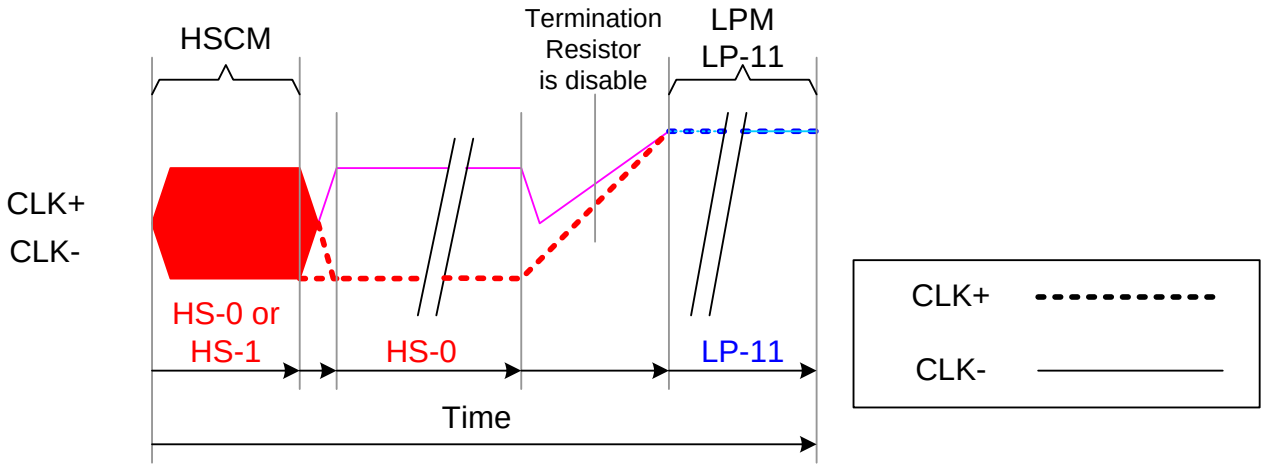


Figure 16 From High Speed Clock Mode (HSCM) to LPM

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All three mode changes are illustrated a flow chart below.

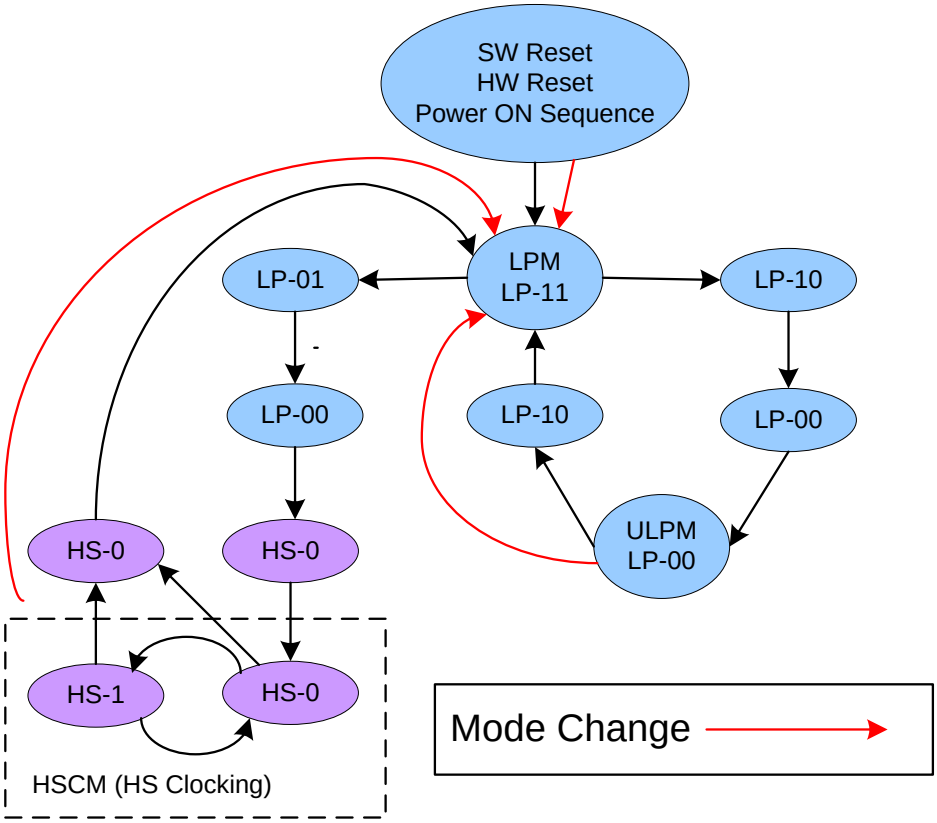


Figure 17 All Three Mode Changes to LPM on the Flow Chart

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3.5.6. Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM).

This sequence is illustrated below.

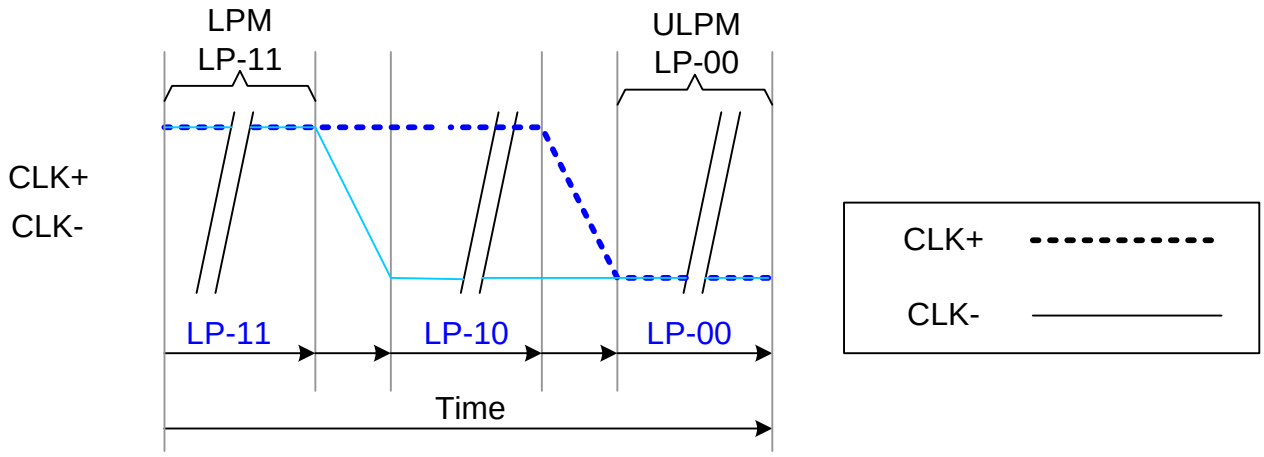


Figure 18 From LPM to ULPM

The mode change is also illustrated below.

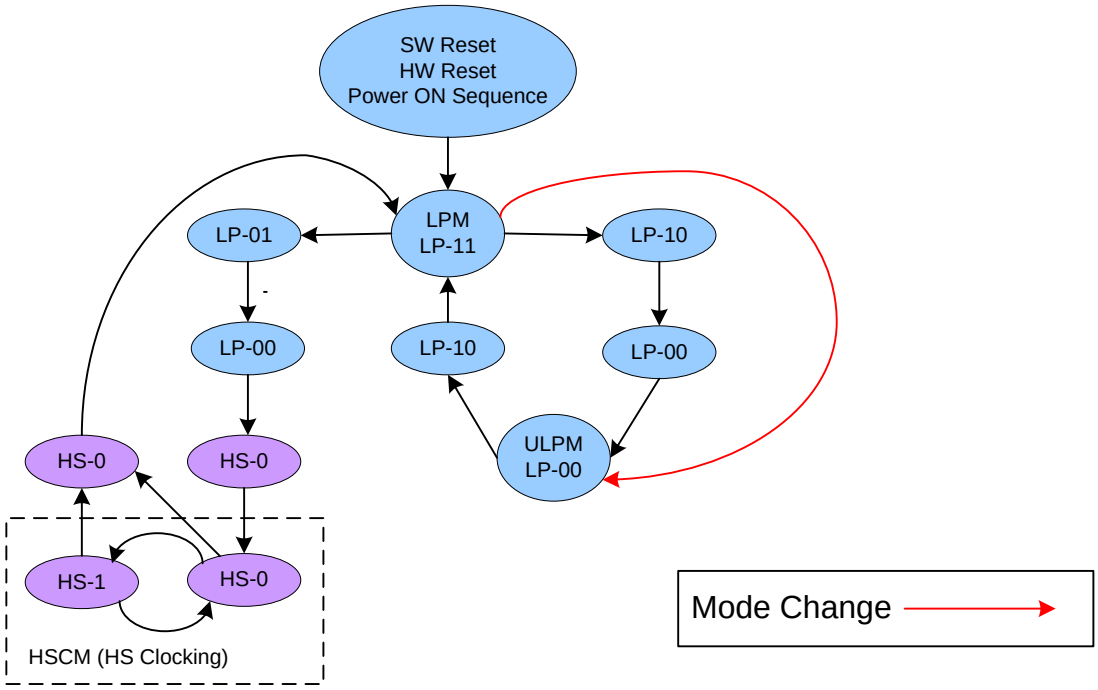


Figure 19 Mode Change from LPM to ULPM on the Flow Chart

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3.5.7. High-Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

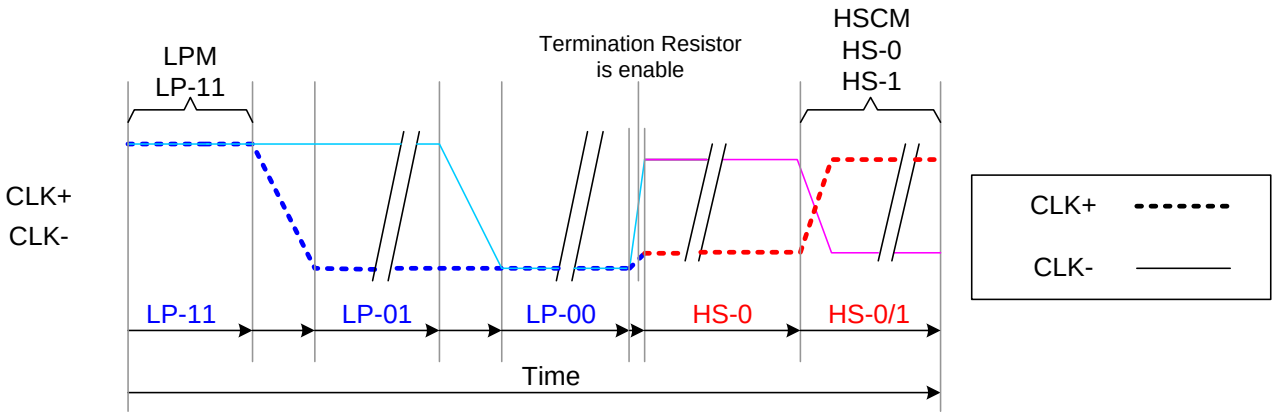


Figure 20 From LPM to HSCM

The mode change is also illustrated below.

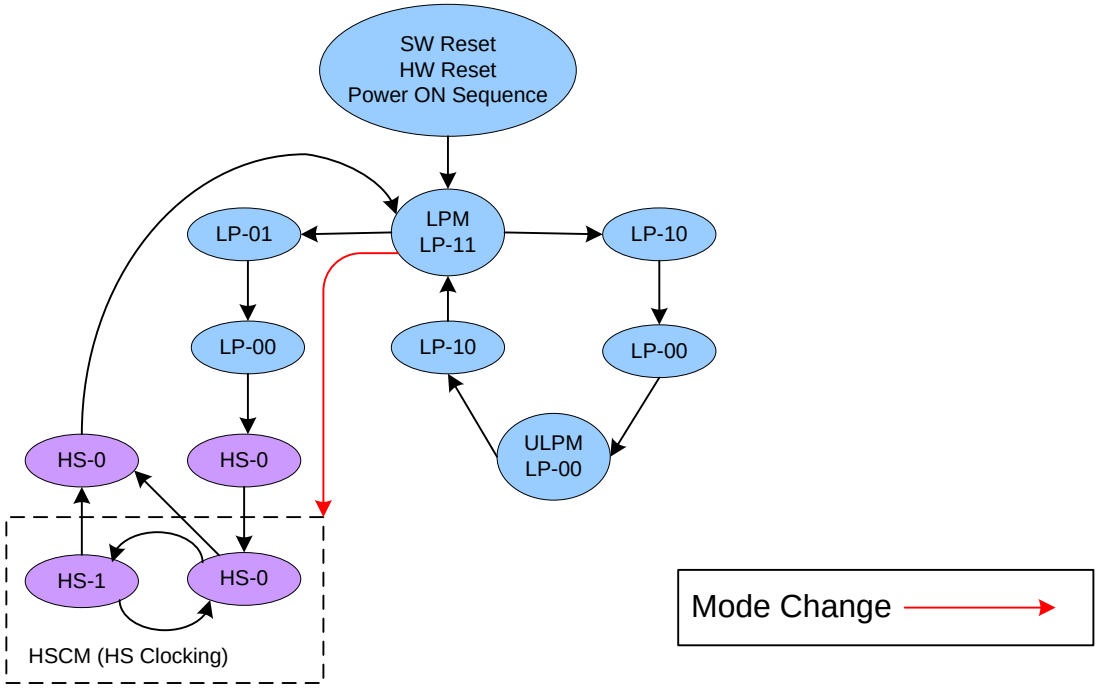


Figure 21 Mode Change from LPM to HSCM on the Flow Chart

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The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-D1+/- or DSI-D0+/- lanes.

The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

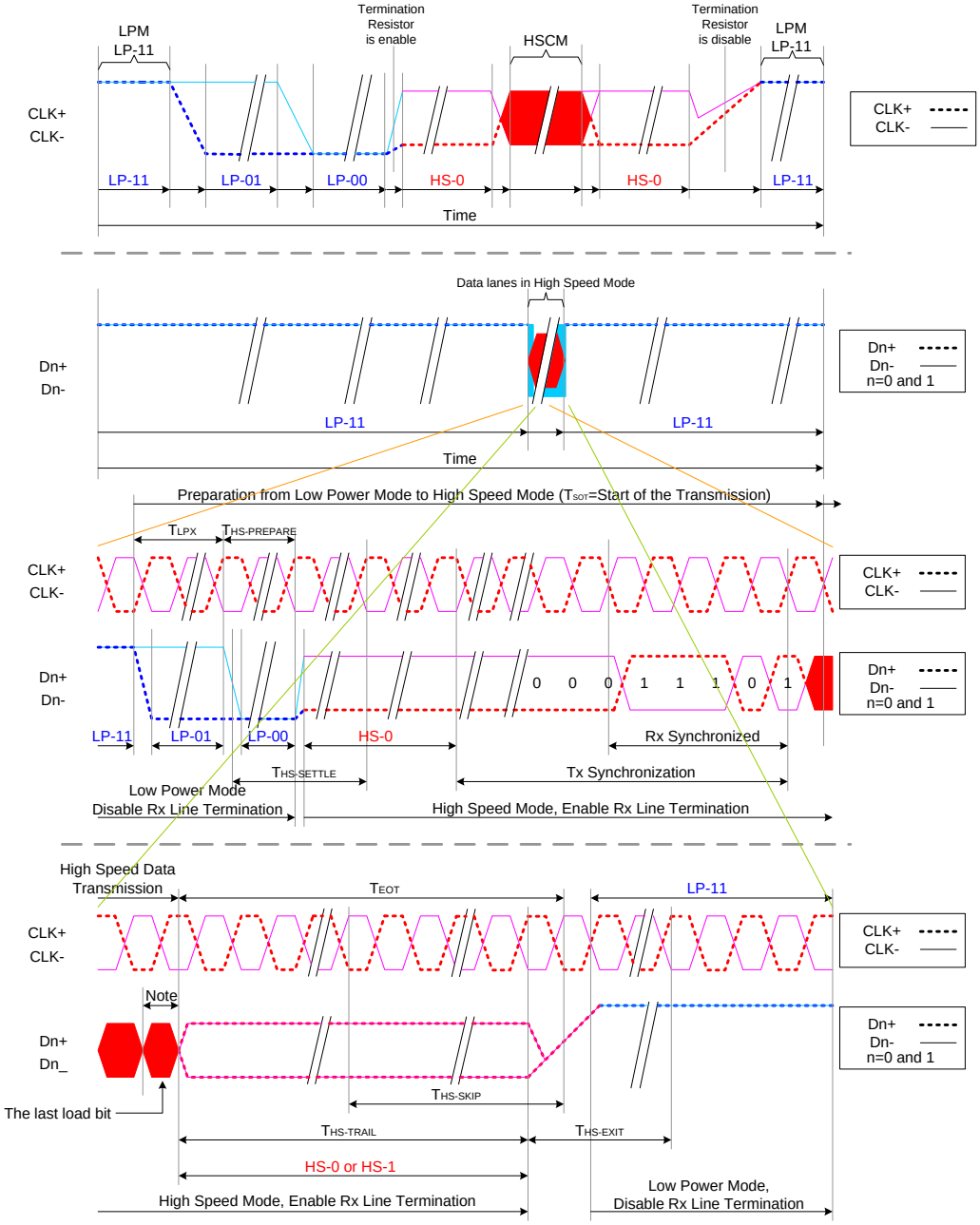


Figure 22 High Speed Clock Burst[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

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3.5.8. DSI-D1 and DSI-D0 Data Lanes

3.5.9. General

DSI-D1+/- and DSI-D0+/- Data Lanes can be driven in different modes which are:

- Escape Mode (Only DSI-D0+/- data lanes are used)
- High-Speed Data Transmission (DSI-D1+/- and DSI-D0+/- data lanes are used)
- Bus Turnaround Request (Only DSI-D0+/- data lanes are used)

These modes and their entering codes are defined on the following table.

Table 11 Entering and Leaving Sequences[Note]

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

Note 1. DSI-D1+/- and DSI-D0+/- data lanes are used.
2. More information on chapter "Bus Turnaround ".

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3.5.10. Escape Modes

DSI-D0+/- data lanes can be used in different Escape Modes when data lanes are in Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MPU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which is resetting the display module,
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MPU.

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0-= 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:

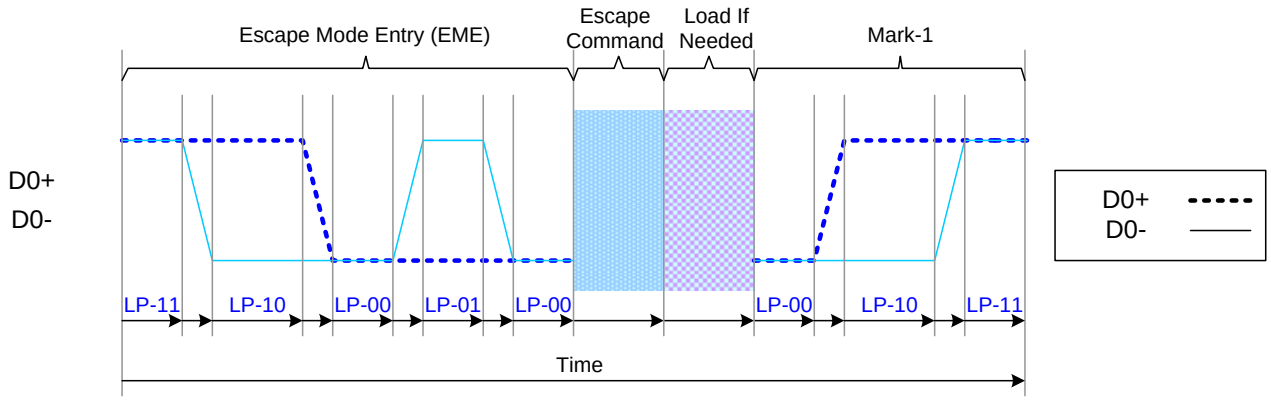


Figure 23 General Escape Mode Sequence

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There are a total of eight Escape Commands (EC) divided into two types, Modes and Triggers, see Table 12: Escape Commands.

An example of a Mode type Escape Command is 'Ultra-Low Power Mode' where the MPU instructs the display module to enter it's Ultra-Low Power Mode.

Escape commands are defined on the next table.

Table 12 Escape Commands[Note]

Escape command	Command Type Mode / Trigger	Entry command Pattern (First Bit ➔ Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, Note 1	Mode	1001 1111 b	-	-
Undefined-2, Note 1	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Uknown-5, Note 1	Trigger	1010 0000 b	-	-

Note *1. This Escape command support has not been implemented on the display module.*
2. n = 1
3. x = Supported
4. - = Not Supported

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3.5.11. Low-Power Data Transmission (LPDT)

The MPU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MPU.

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
  - One or more bytes (8 bit)
  - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

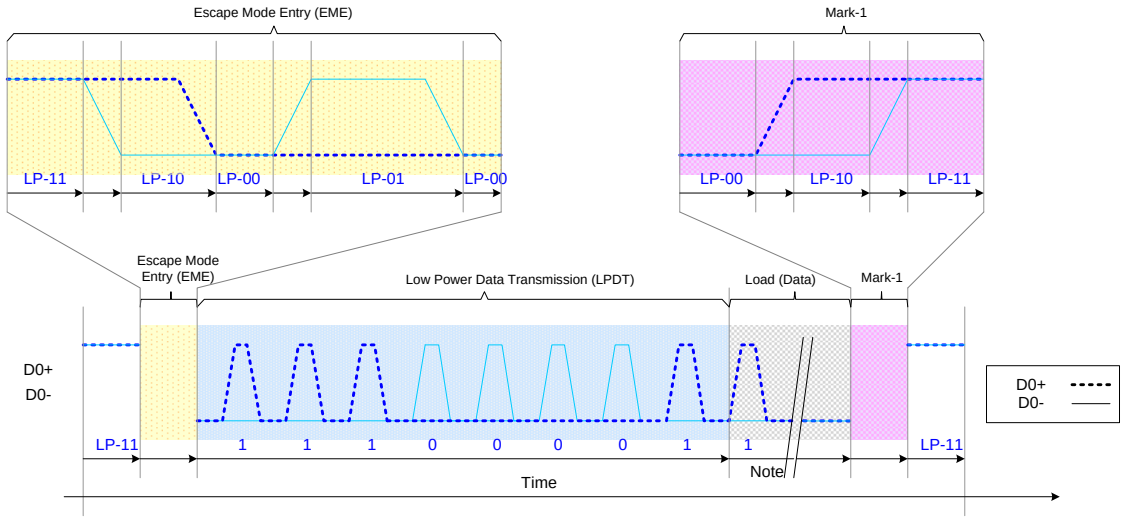


Figure 24 Low-Power Data Transmission (LPDT)[Note]

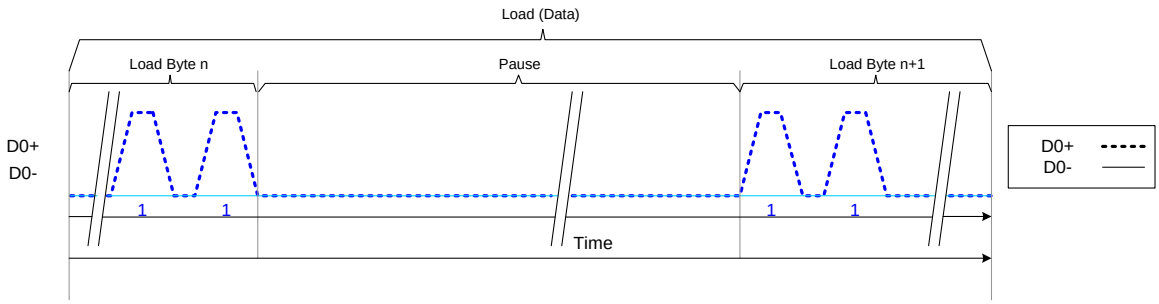


Figure 25 Pause (Example)

Note Load (Data) is presenting that the first bit is logical '1' in this example.

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3.5.12. Ultra-Low Power State (ULPS)

The MPU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MPU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

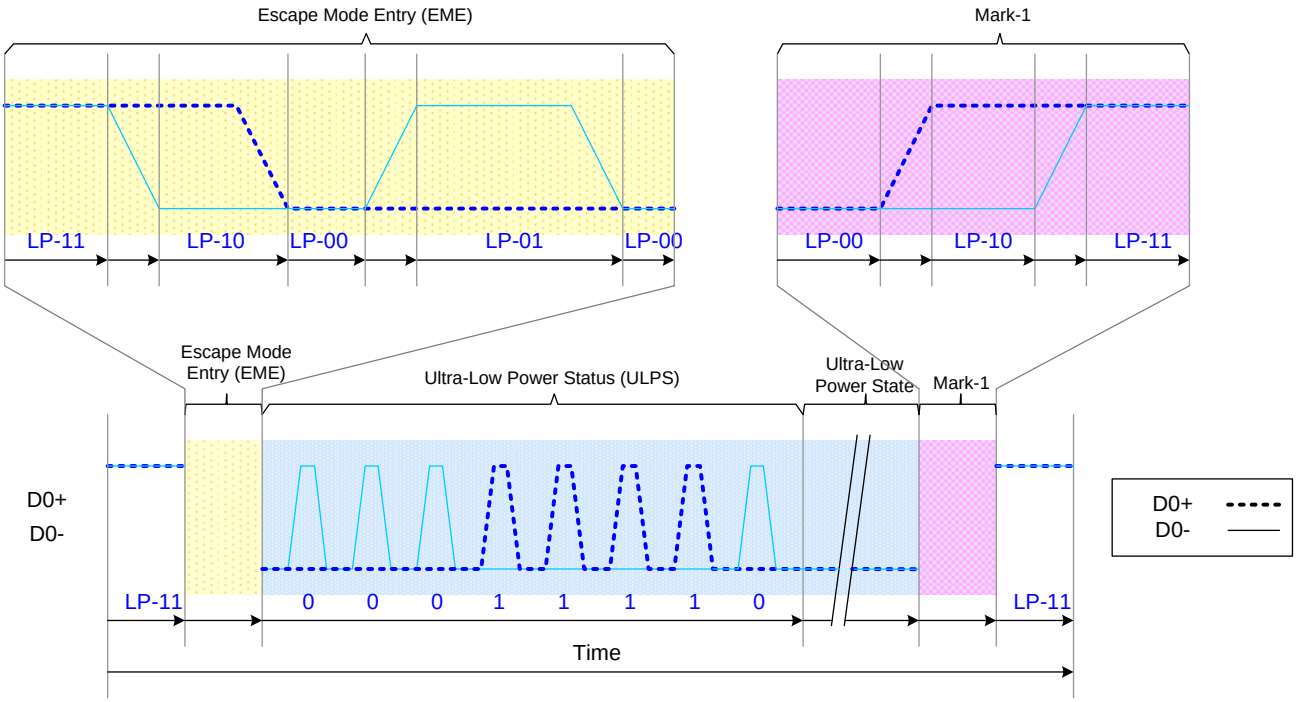


Figure 26 Ultra-Low Power State (ULPS)

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3.5.13. Remote Application Reset (RAR)

The MPU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

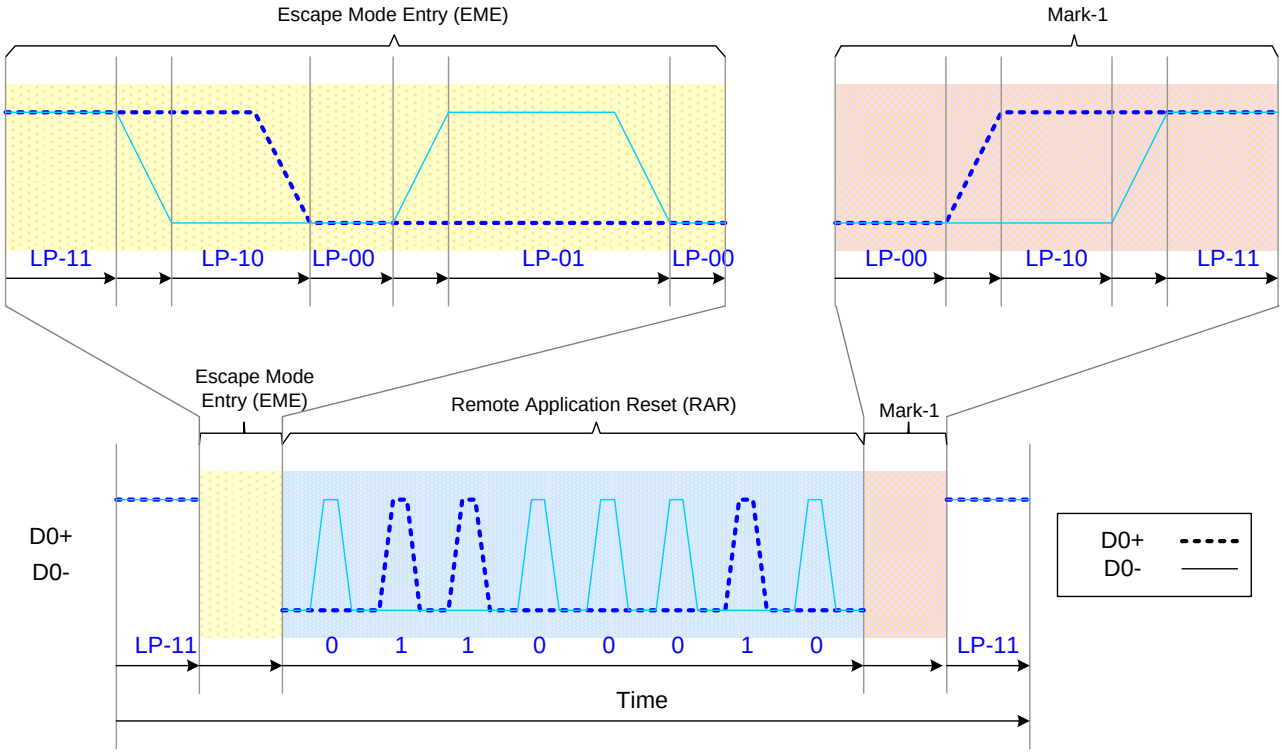


Figure 27 Remote Application Reset (RAR)

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3.5.14. Acknowledge (ACK)

The display module can inform to the MPU when an error has not recognized on it by Acknowledge (ACK).

The display module is sending the Acknowledge (ACK) what is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

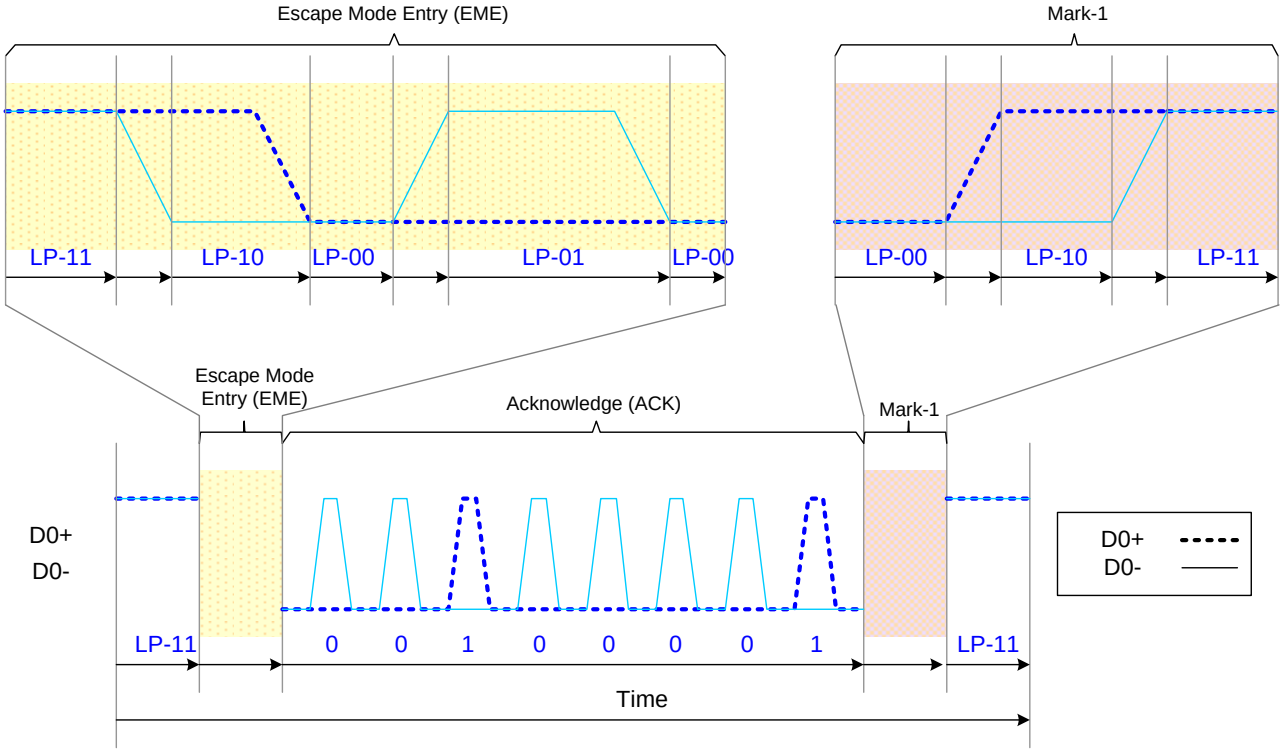


Figure 28 Acknowledge (ACK)

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3.5.15. High-Speed Data Transmission (HSDT)

3.5.16. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MPU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MPU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below

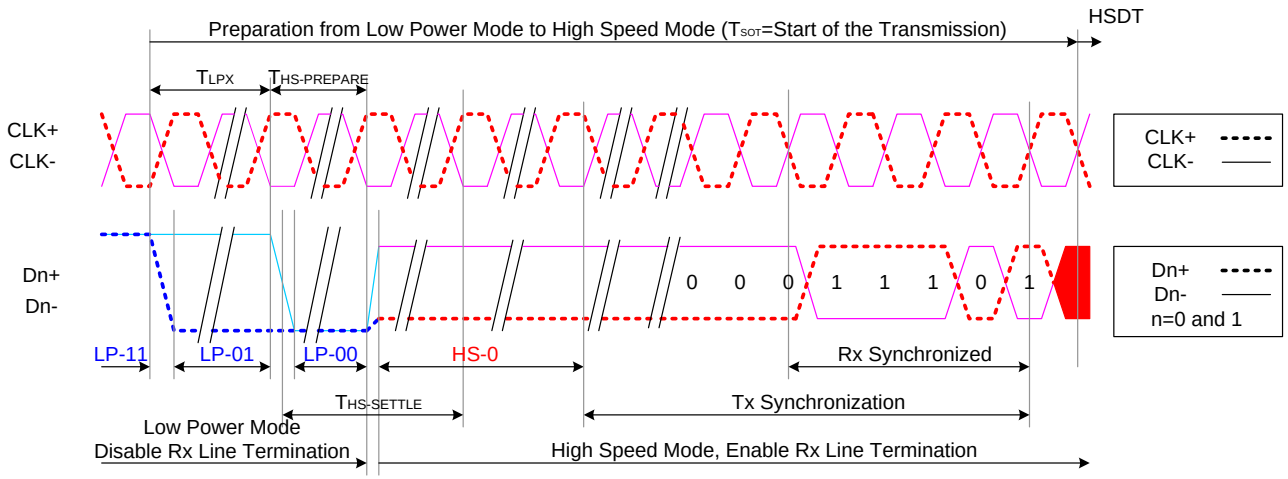


Figure 29 Entering High-Speed Data Transmission (TSOT of HSDT)

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3.5.17. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MPU and this HSCM is kept until data lanes DSI-D1+/- and DSI-D0+/- are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D1+/- and DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - o MPU changes to HS-1, if the last load bit is HS-0
  - o MPU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

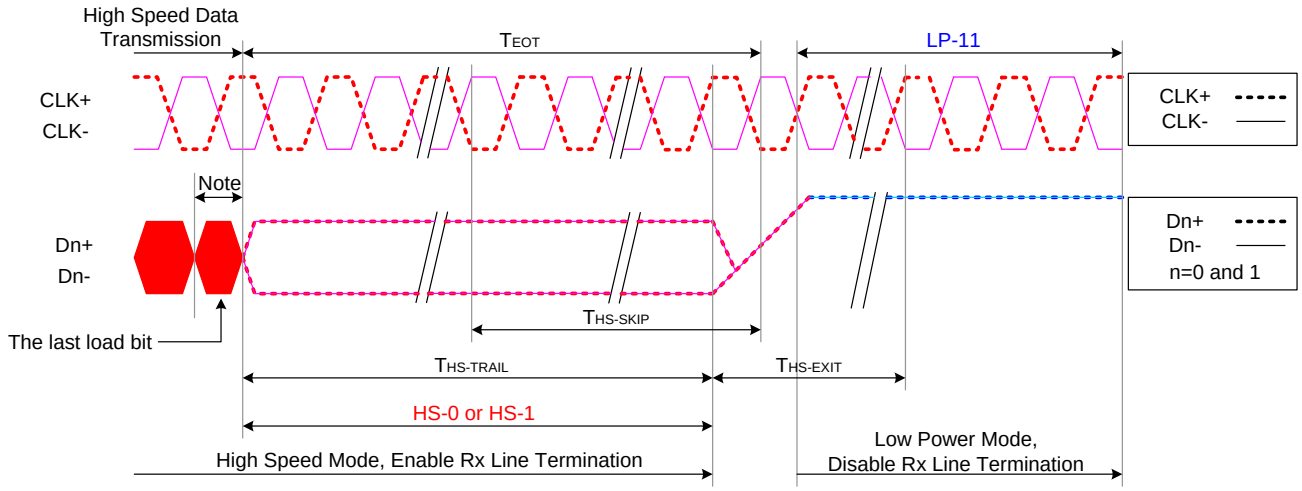


Figure 30 Leaving High-Speed Data Transmission (TEOT of HSDT)[Note]

Note 1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

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3.5.18. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one data packet or several data packets.

These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

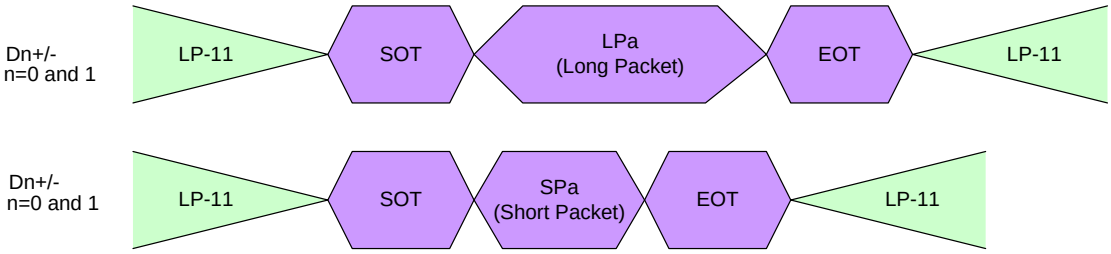


Figure 31 Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission is illustrated for reference purposes below:

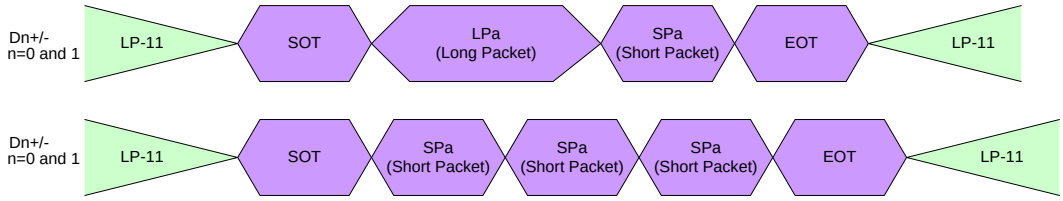


Figure 32 Multiple Packets in High-Speed Data Transmission – Examples

Table 13 Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

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Byte orders of the sent packet is in High-Speed Data Transmission (HSDT) as follows.

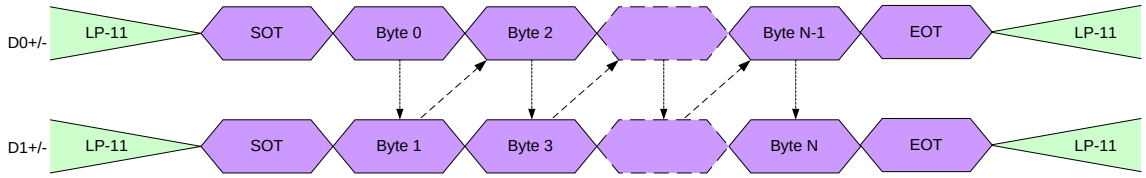


Figure 33 Single Packet in HSDT – Even Number of Bytes

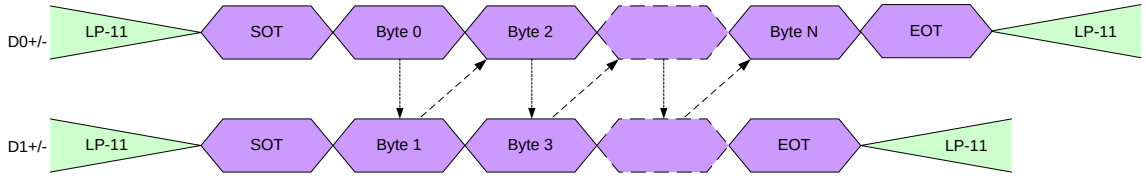


Figure 34 Single Packet in HSDT – Odd Number of Byte

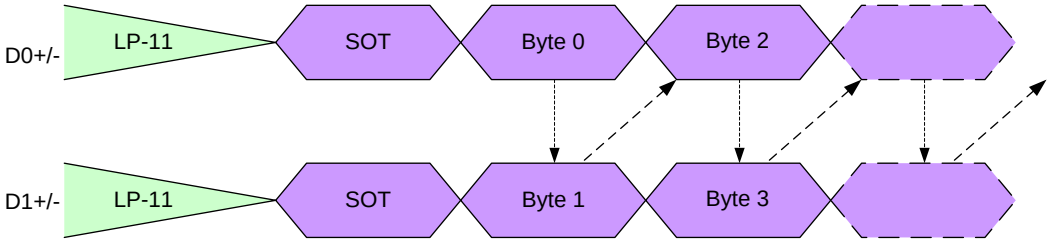


Figure 35 Start of Transmission (SoT) in HSDT for Multiple Packets

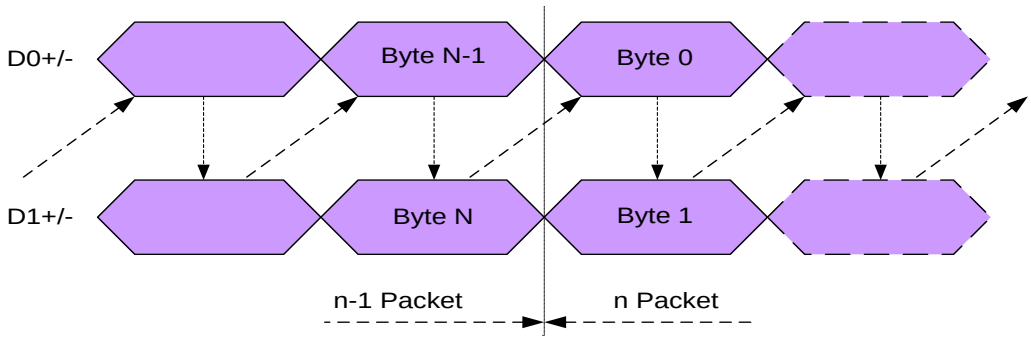


Figure 36 Continue Multiple Packets in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

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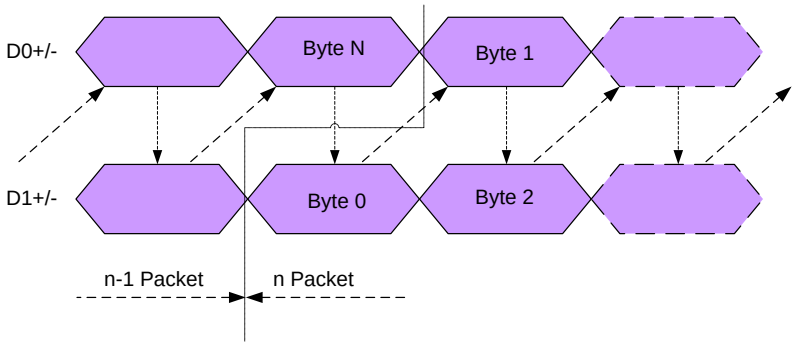


Figure 37 Continue Multiple Packets in HSDT when Number of Bytes is not Equal on Both Data Lanes at the End of the Packet

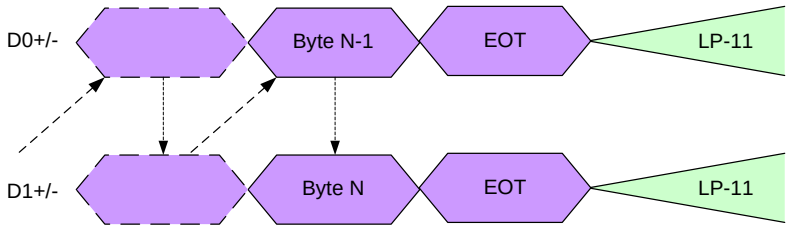


Figure 38 End of Transmission (EoT) in HSDT when Number of Bytes is Equal on Both Data Lanes at the End of the Packet

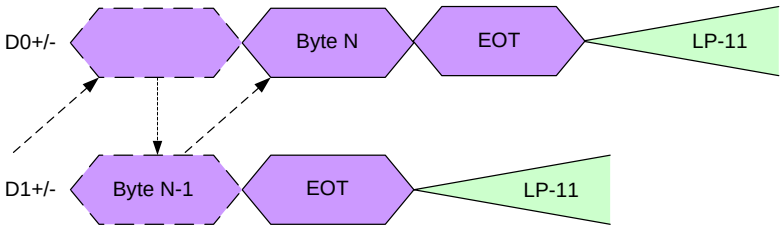


Figure 39 End of Transmission (EoT) in HSDT when Number of Bytes is not Equal on Both Data Lanes at cthe End of the Packet

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3.5.19. Bus Turnaround (BTA)

The MPU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MPU or display module.

The MPU and display module are using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MPU wants to do the bus turnaround procedure to the display module, as follows.

- Start (MPU): LP-11
- Turnaround Request (MPU): LP-11 =>LP-10 =>LP-00 => LP-10 => LP-00
- The MPU waits until the display module is starting to control DSI-D0+/- data lanes and the MPU stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MPU to the display module) is illustrated below

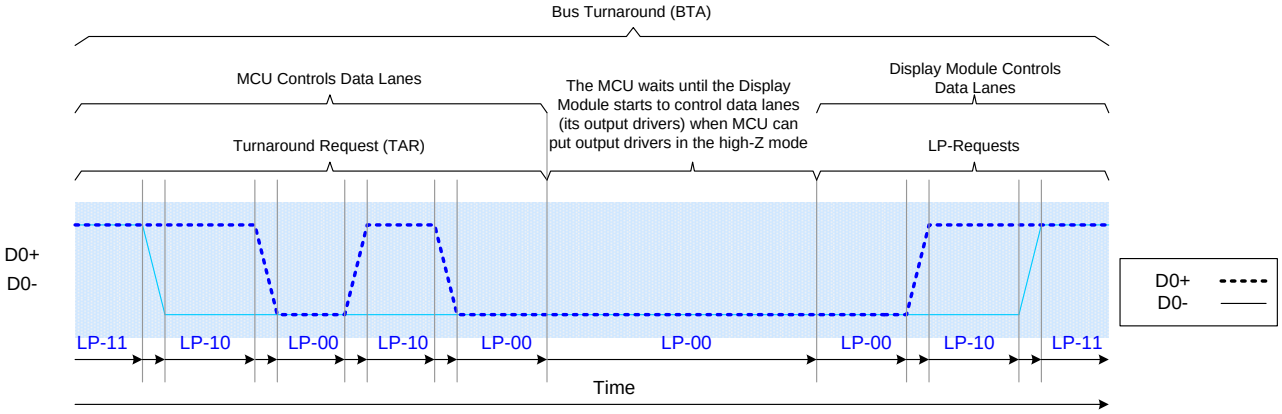


Figure 40 Bus Turnaround Procedure

MPU and display module terms are switched on the Figure 40, if the Bus Turnaround (BTA) is from the display module to the MPU.

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3.5.20. Packet Level Communication

3.5.21. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes[Note].

The lengths of the packets are

• Short Packet (SPa): 4 bytes

• Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

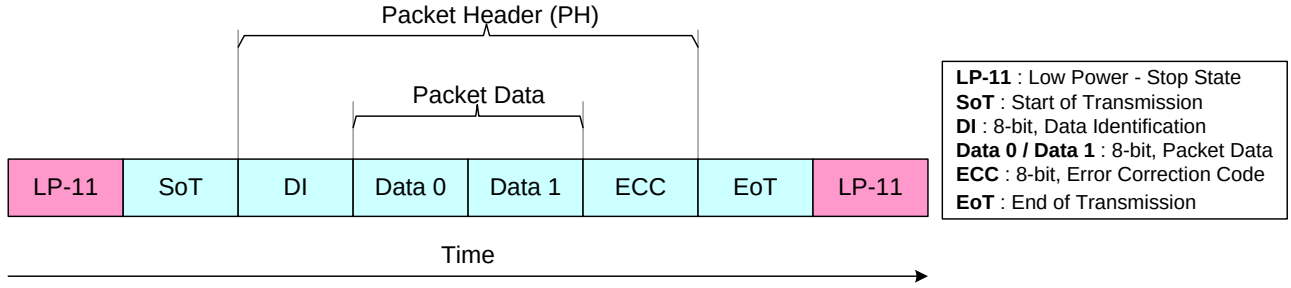


Figure 41 Short Packet (SPa) Structure

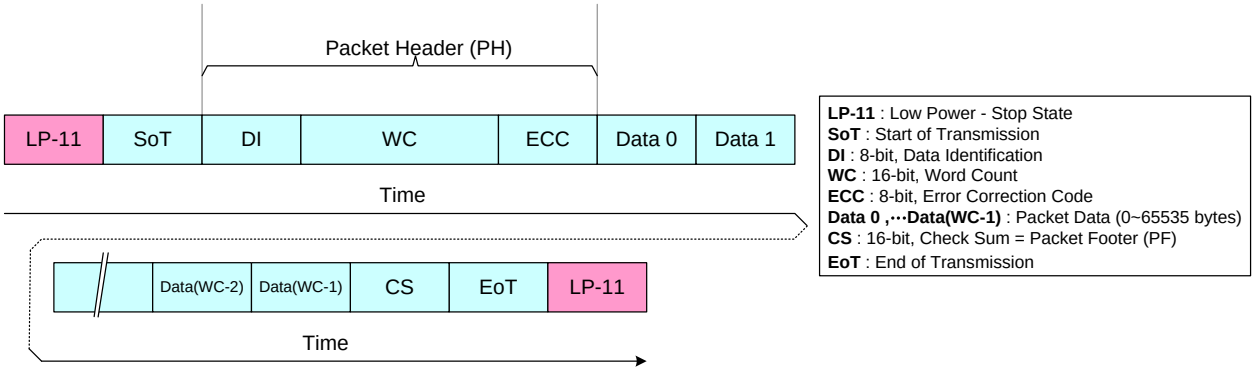


Figure 42 Long Packet (LPa) Structure

Note *Short Packet (SPa) and Long Packet (LPa) are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).*
The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

- *LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11*
- *LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11*
- *LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11*

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3.5.22. Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

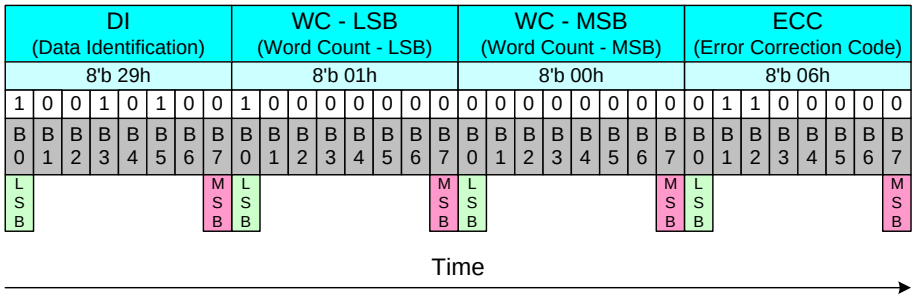


Figure 43 Bit Order of the Byte on Packets

3.5.23. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

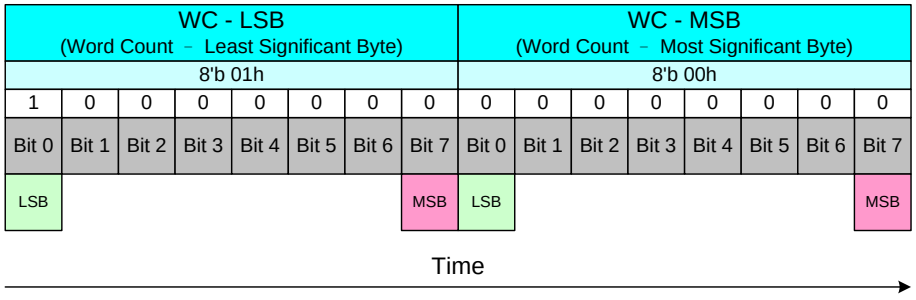


Figure 44 Byte Order of the Multiple Byte Information on Packets

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3.5.24. Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

• 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)

• 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1

• 4th byte: Error Correction Code (ECC)

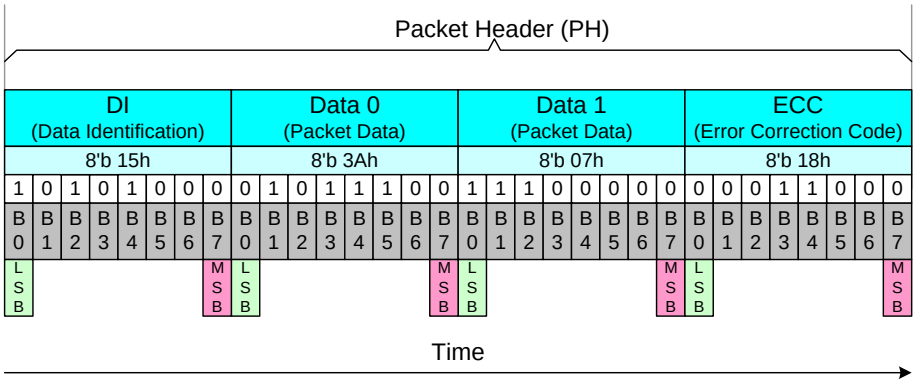


Figure 45 Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

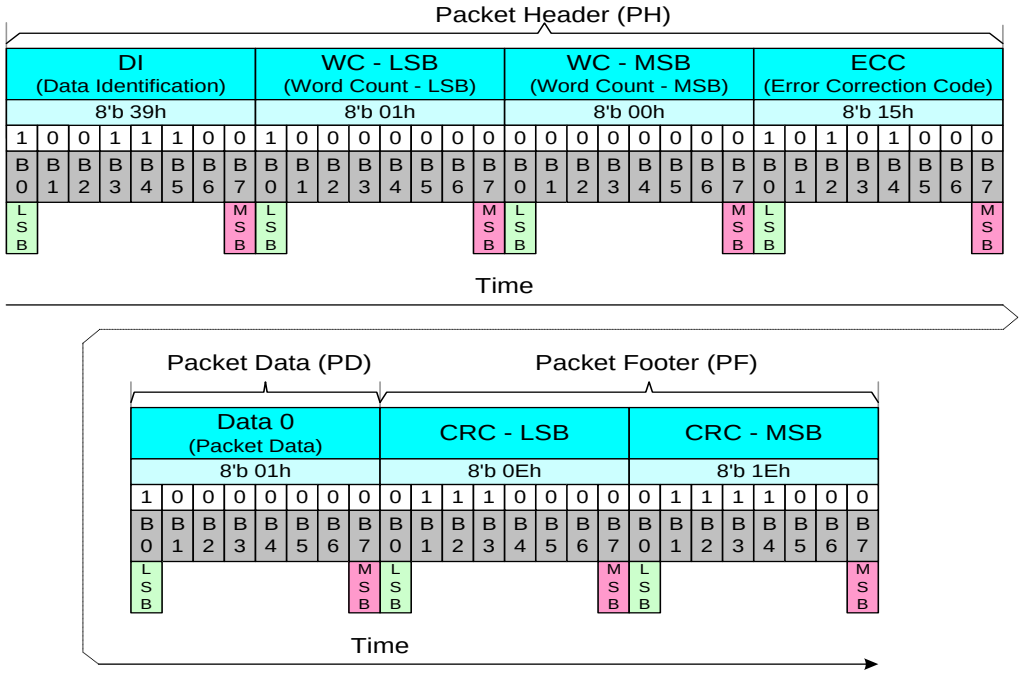


Figure 46 Packet Header (PH) on Long Packet (LPa)

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3.5.25. Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated, see figure below.

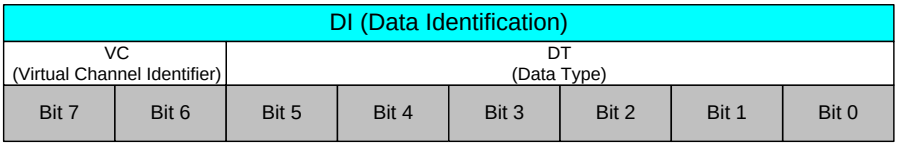


Figure 47 Data Identification (DI) Structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

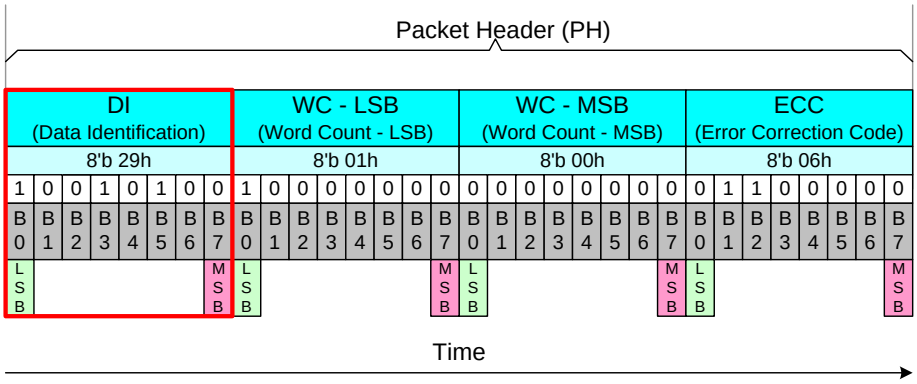


Figure 48 Data Identification (DI) on the Packet Header (PH)

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3.5.26. Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MPU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

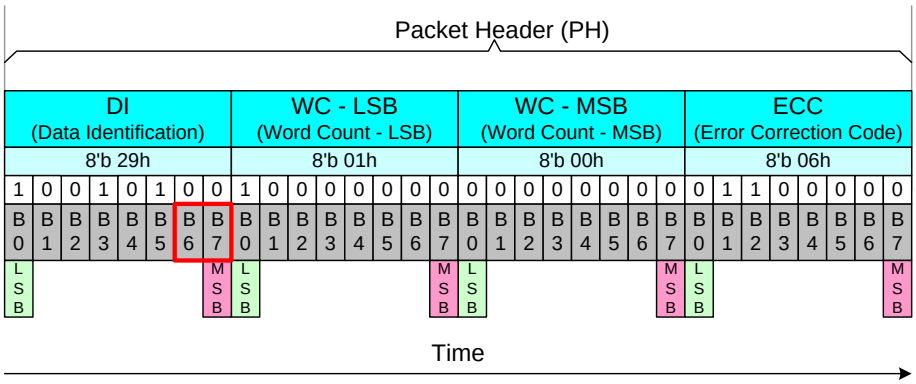


Figure 49 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules.

Devices are using the same virtual channel what the MPU is using to send packets to them e.g.

- The MPU is using the virtual channel 0 when it sends packets to this display module
- This display module is also using the virtual channel 0 when it sends packets to the MPU

This functionality is illustrated below.

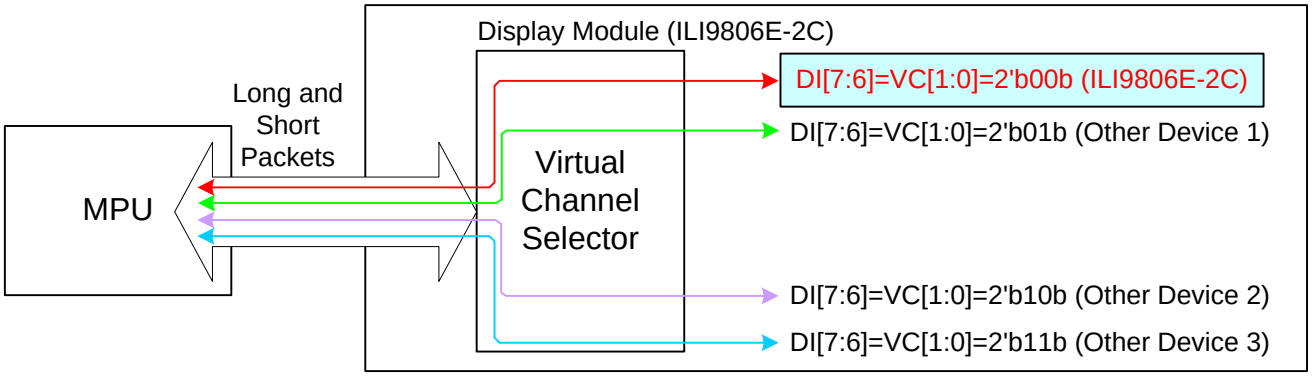


Figure 50 Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI[7..6]=VC[1..0]=00_b) when the MPU is sending “End of Transmission Packet” to the display module. See chapter “End of Transmission Packet (EoTP)”.

This display module is not supporting the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC[1..0]) is 00b for this display module.

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3.5.27. Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

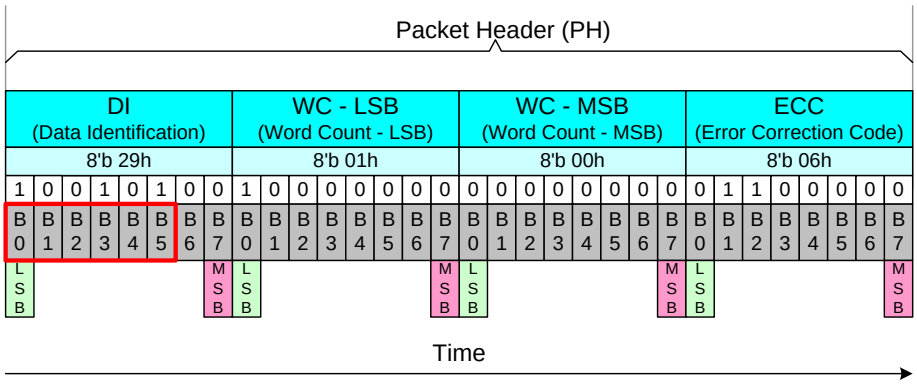


Figure 51 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa).

Data Types (DT) are different from the MPU to the display module (or other devices) and vice versa.

These Data Type (DT) are defined on tables below.

Table 14 Data Type (DT) from the MPU to the Display Module (ILI9806E-2C)

From the MPU to the Display Module (**ILI9806E-2C**)									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	1	0	0	0	08	End of Transmission Packet, Note 1	SPa (Short Packet)	EoTP
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)	DCSWN-S
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)	DCSW1-S
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)	DCSRN-S
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)	SMRPS-S
0	0	1	0	0	1	09	Null Packet, No Data, Note 2	LPa (Long Packet)	NP-L
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)	DCSW-L

Note 1 This can be used when the MPU wants to secure that there is the end of the transmission in High Speed Data Transferring (HSDT) mode.

Note 2 This can be used when data lanes are wanted to keep in High Speed Data Transferring (HSDT) Mode.

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Table 15 Data Type (DT) from the Display Module (ILI9806E-2C) to the MPU

From the Display Module (**ILI9806E-2C**) to the MPU									
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet	Abbreviation
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)	AwER
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)	DCSRR-L
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)	DCSRR1-S
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)	DCSRR2-S

The receiver is ignored other Data Type (DT) if they are not defined on tables: “ Table 14 Data Type (DT) from the MPU to the Display Module (or Other Devices)” or “ Table 15 Data Type (DT) from the Display Module (or Other Devices) to the MPU”.

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3.5.28. Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

• Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI(Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

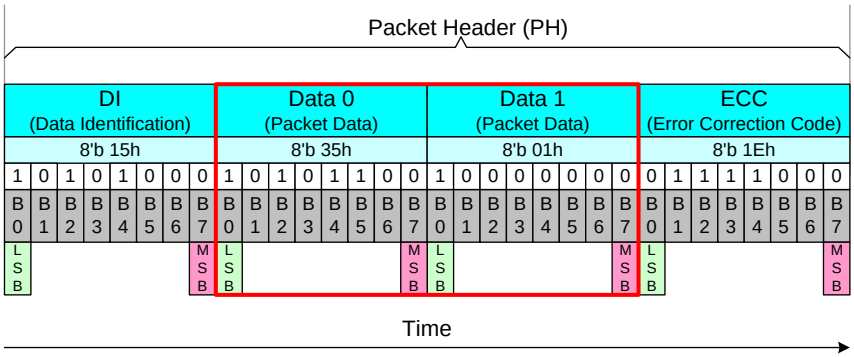


Figure 52 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI(Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

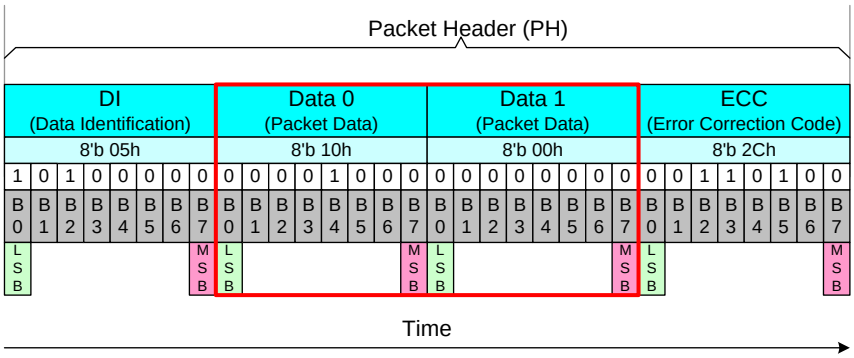


Figure 53 Packet Data (PD) for Short Packet (SPa), 1 Byte Information

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3.5.29. Word Count (WC) on the Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

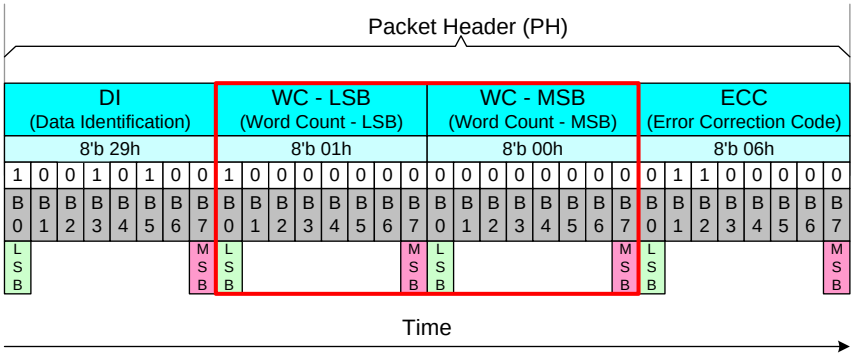


Figure 54 Word Count (WC) on the Long Packet (LPa)

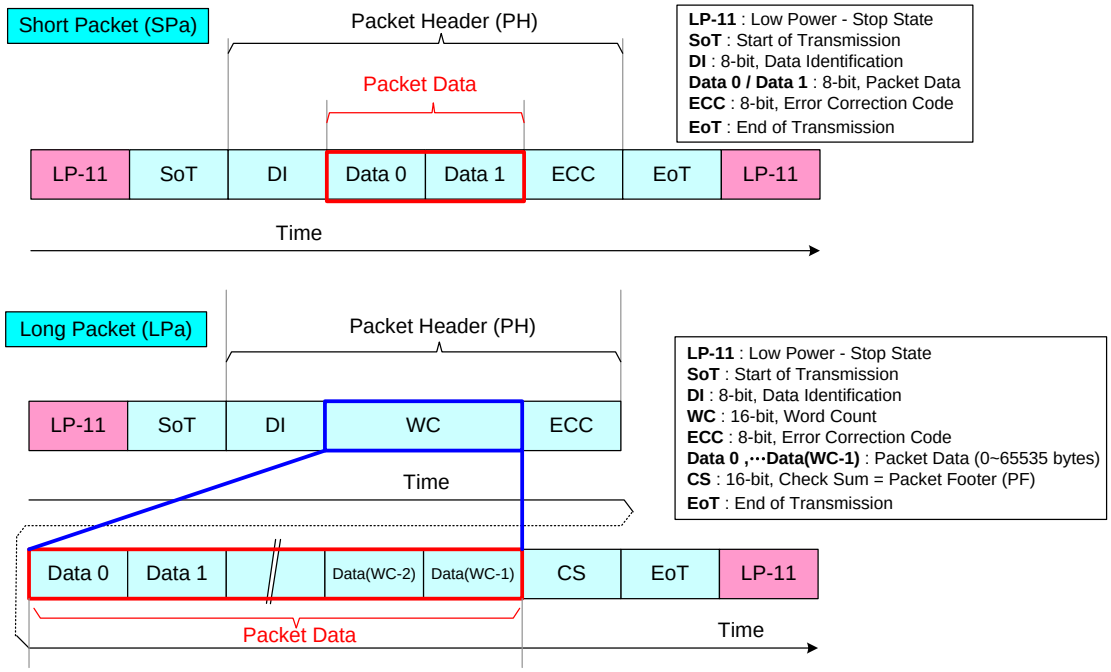


Figure 55 Packet Data in Short and Long Packets

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3.5.30. Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors.

The ECC protects the following fields:

• Short Packet (SPa): Data Identification (DI) byte (8 bits: D[0…7]), Packet Data (PD) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

• Long Packet (LPa): Data Identification (DI) byte (8 bits: D[0…7]), Word Count (WC) bytes (16 bits: D[8…23]) and ECC (8 bits: P[0…7])

D[23…0] and P[7…0] are illustrated for reference purposes below.

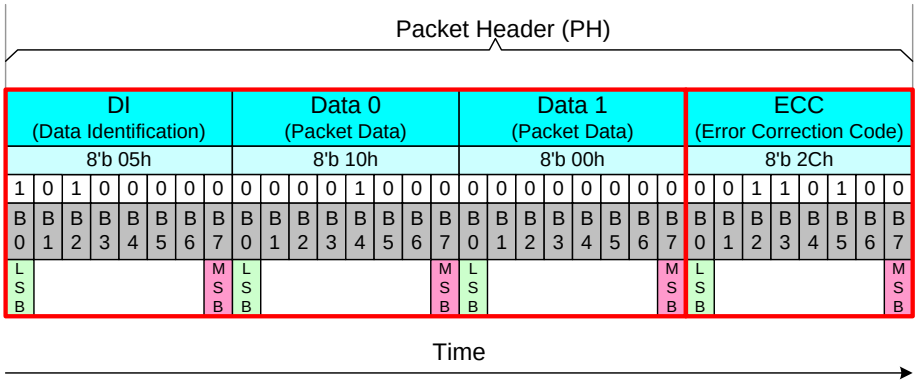


Figure 56 D[23…0] and P[7…0] on the Short Packet (SPa)

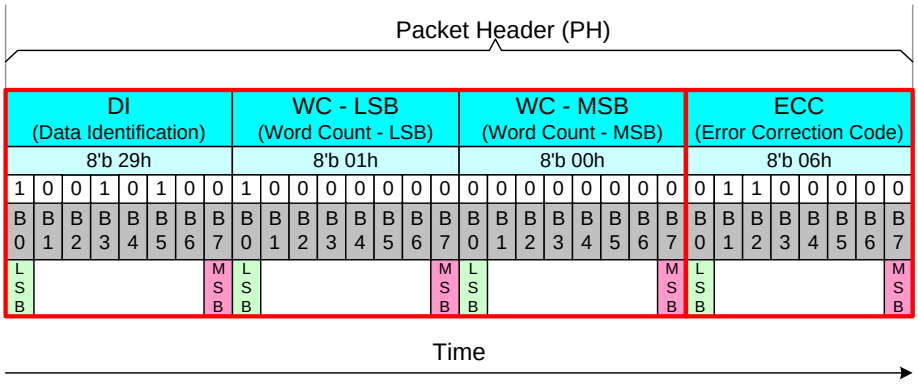


Figure 57 D[23…0] and P[7…0] on the Long Packet (LPa)

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Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

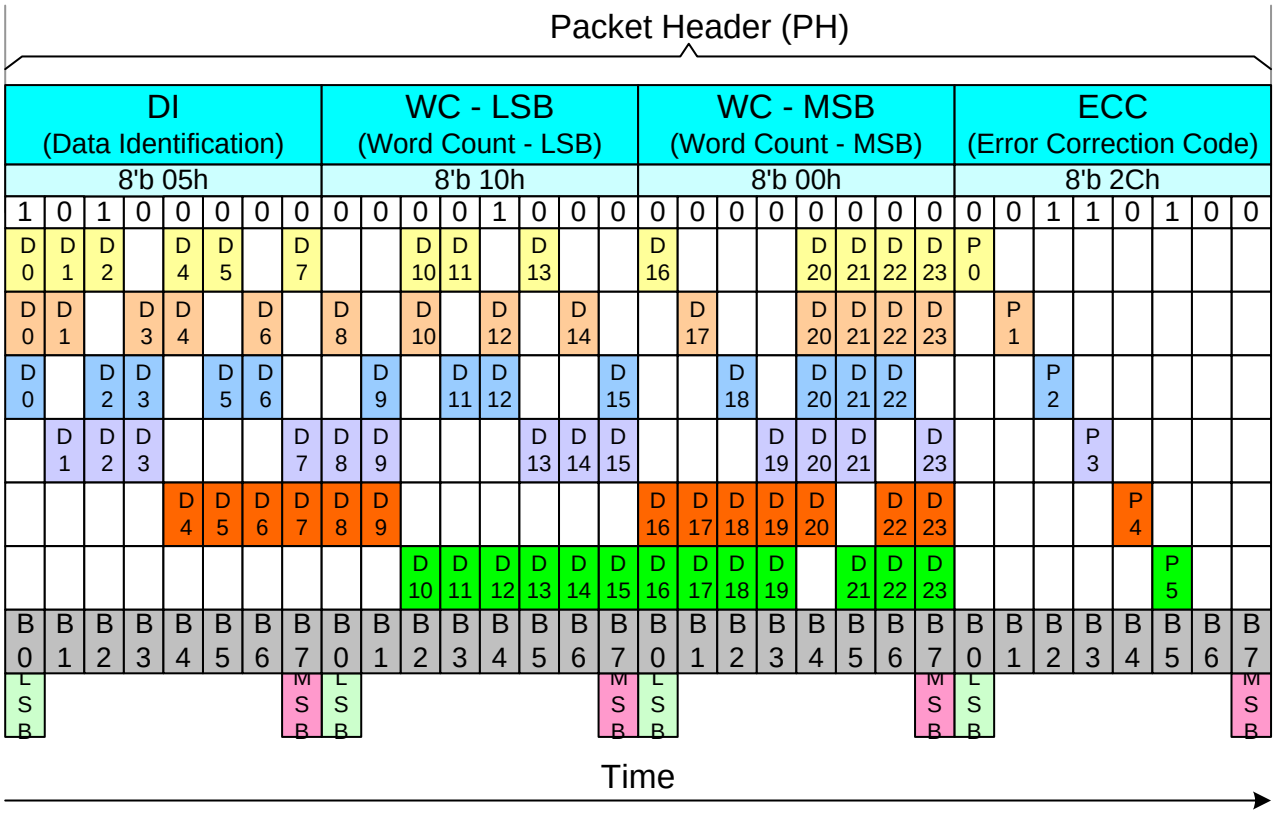


Figure 58 XOR Functionality on the Short Packet (SPa)

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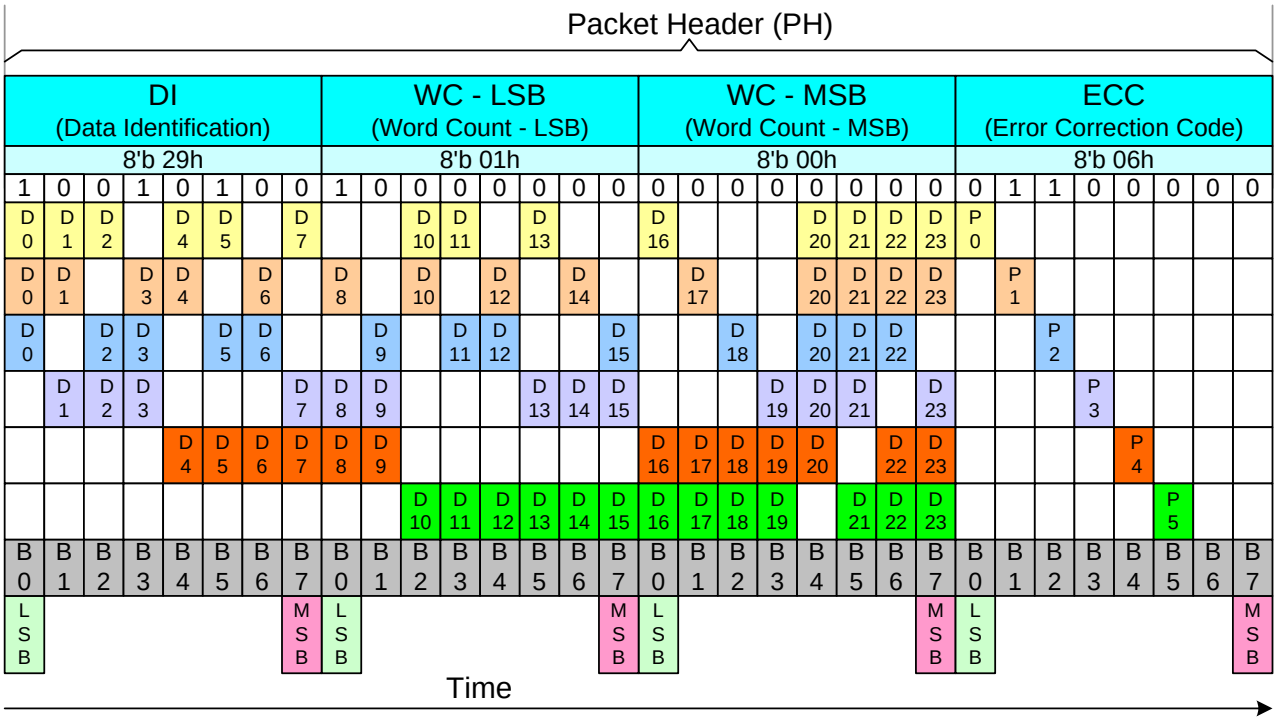


Figure 59 XOR Functionality on the Long Packet (LPa)

The transmitter (The MPU or the Display Module) is sending data bits D[23…0] and Error Correction Code (ECC) P[7…0]. The receiver (The Display module or the MPU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7…0].

This functionality, where the transmitter is the MPU and the receiver is the display module, is illustrated for reference purposes below.

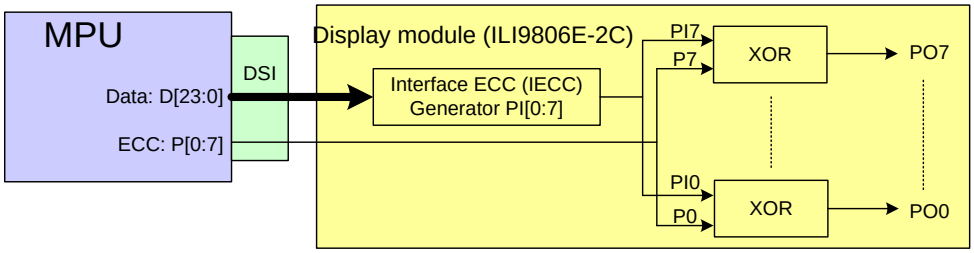


Figure 60 Internal Error Correction Code (IECC) on the Display Module (The Receiver)

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The sent data bits (D[23…0]) and ECC (P[7…0]) are received correctly, if a value of the PO[7…0]) is 00h.

The sent data bits (D[23…0]) and ECC (P[7…0]) are not received correctly, if a value of the PO[7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 61 Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 62 Internal XOR Calculation between ECC and IECC Values - Error

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The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23…0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7…0] is compared to values on the following table.

Table 16 One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7…0] is on Table 25: One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

• PO[7…0] = 0Eh

• The bit of the data (D[23…0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7…0] is not on Table 25: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7…0] = 0Ch.

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3.5.31. Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa).

The number of the data bytes is defined on chapter “Word Count (WC) on the Long Packet (LPa)”.

3.5.32. Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa).

The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

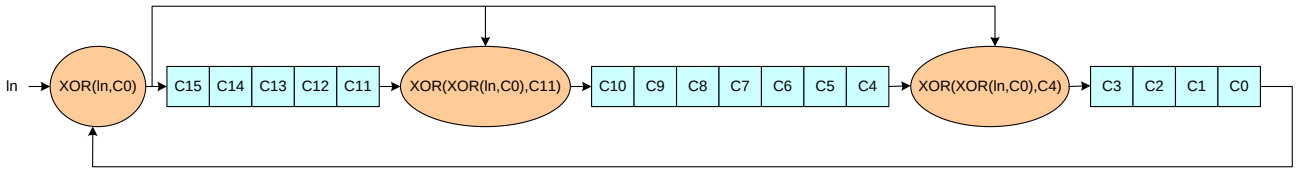
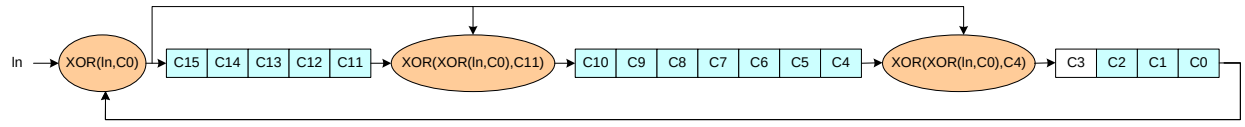


Figure 63 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 64 CRC Calculation – Packet Data (PD) is 01h

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A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.

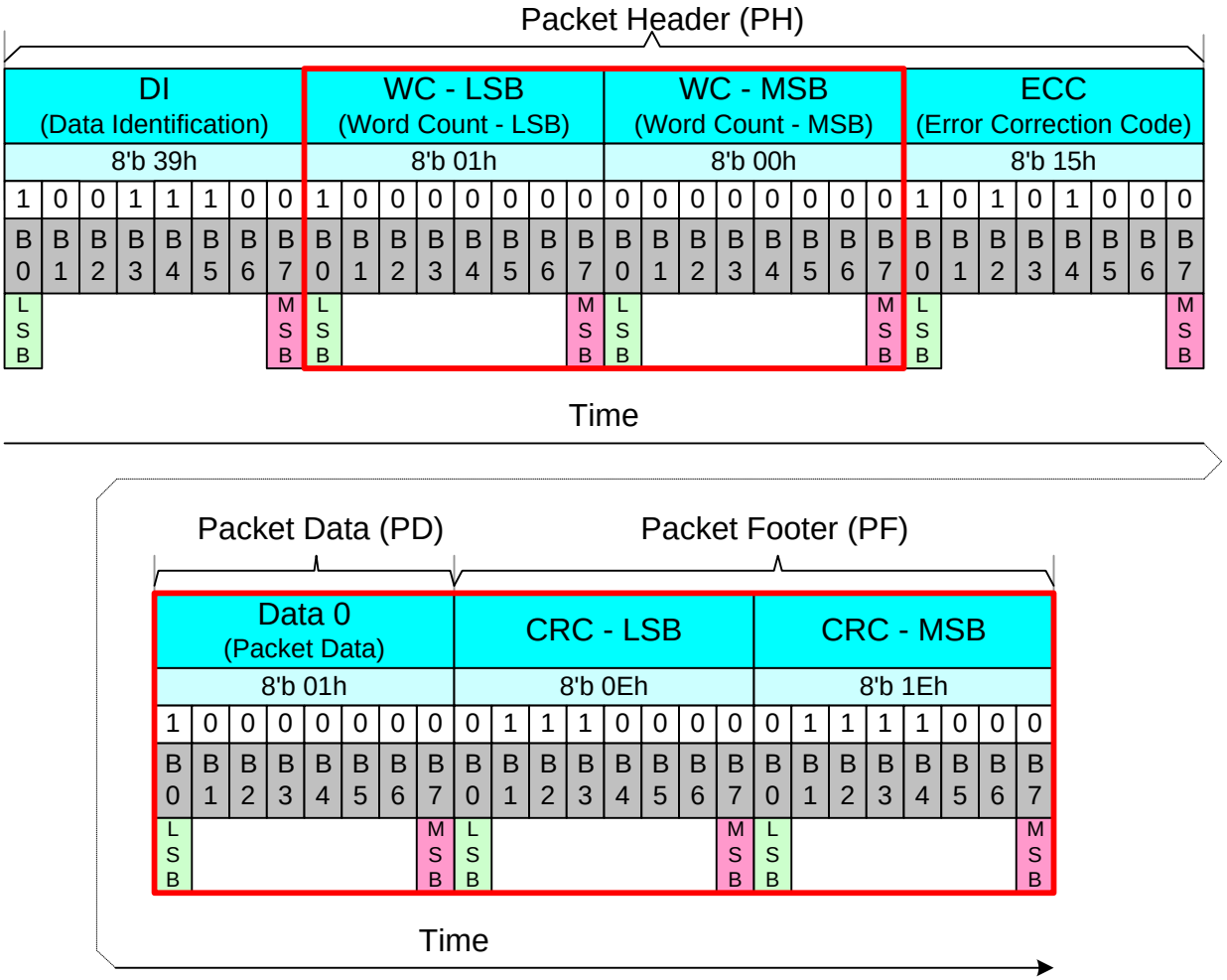


Figure 65 Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

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3.5.33. Packet Transmissions

3.5.34. Packet from the MPU to the Display Module

3.5.35. Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “5.2. Command Description” is used from the MPU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

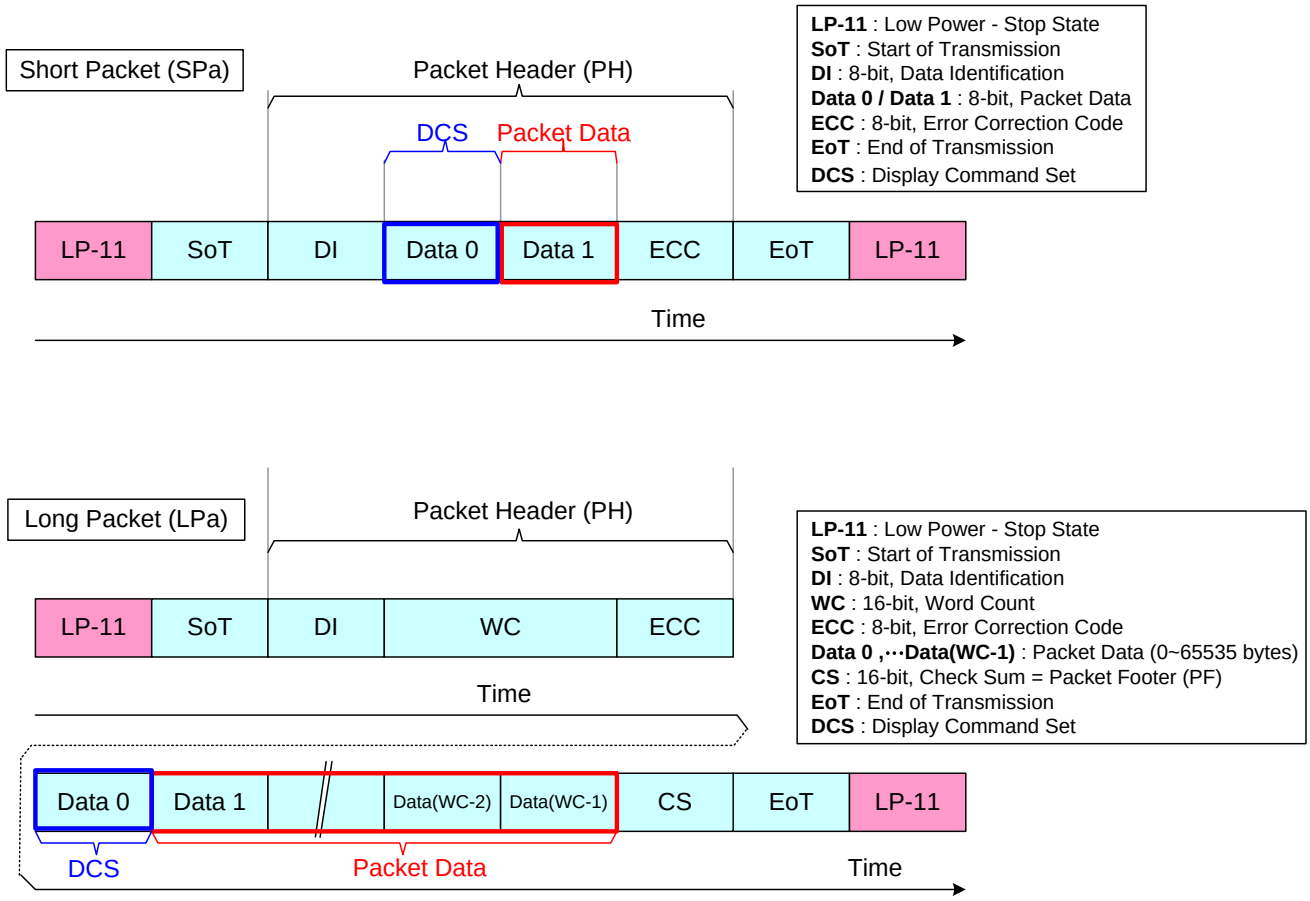


Figure 66 Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

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3.5.36. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MPU to the display module. These commands are defined on a table below. (See chapter "Command Description")

Table 17 Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Page 0 Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

  o Virtual Channel (VC, DI[7…6]): 00b

  o Data Type (DT, DI[5…0]): 00 0101b

• Packet Data (PD)

  o Data 0: "Sleep In (10h)", Display Command Set (DCS)

  o Data 1: Always 00hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

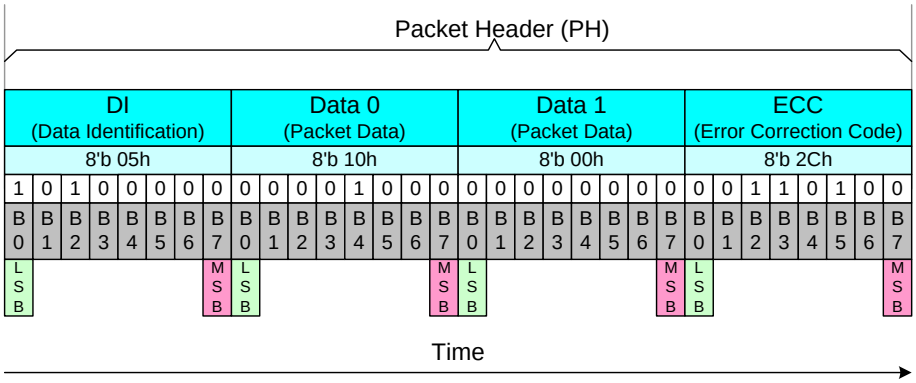


Figure 67 Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

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3.5.37. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MPU to the display module. These commands are defined on a table (See chapter "Command Description") below.

Table 18 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Page 0 Command
Gamma Set (26h)
Interface Pixel Format (3Ah)
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Content Adaptive Brightness control (55h)
Write CABC Minimum Brightness (5Eh)

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 01 0101b

• Packet Data (PD)

o Data 0: "Gamma Set (26h)", Display Command Set (DCS)

o Data 1: 01hex, Parameter of the DCS

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

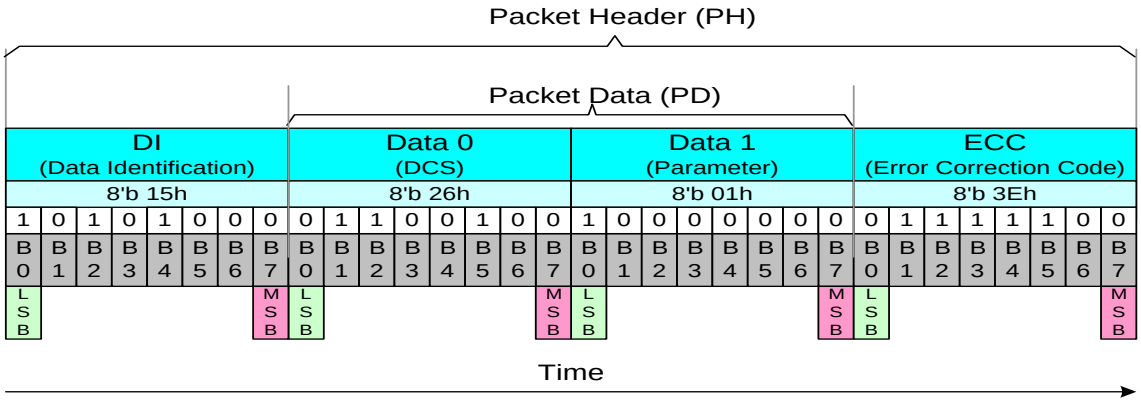


Figure 68 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

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3.5.38. Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MPU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "Command Description") below.

Table 19 Display Command Set (DCS) Write Long (DCSW-L)

Page 0 Command
NOP (00h) , Note 1
Software Reset (01h) , Note 1
Sleep In(10h) , Note 1
Sleep Out (11h) , Note 1
Normal Display Mode On (13h) , Note 1
All Pixel Off (22h)
All Pixel On (23h)
Gamma Set (26h), Note 2
Display Off (28h) , Note 1
Display ON (29h) , Note 1
Interface Pixel Format (3Ah)
Write Display Brightness (51h) , Note 2
Write CTRL Display (53h) , Note 2
Write Content Adaptive Brightness control (55h) , Note 2
Write CABC Minimum Brightness (5Eh)

Note 1 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, No Parameter"

Note 2 Also Short Packet (SPa) can be used; See chapter "Display Command Set (DCS) Write, 1 Parameter"

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Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

• Data Identification (DI)

  o Virtual Channel (VC, DI[7…6]): 00b

  o Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  o Word Count (WC): 0001h

• Error Correction Code (ECC)

• Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

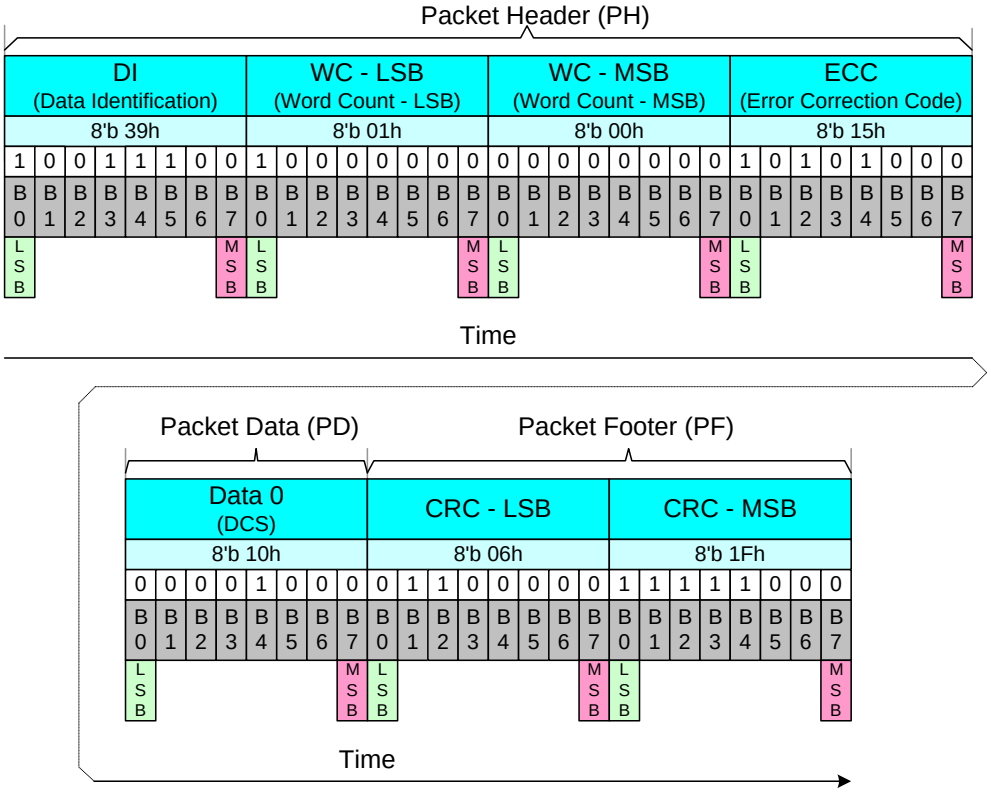


Figure 69 Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

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Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

o Word Count (WC): 0002h

• Error Correction Code (ECC)

• Packet Data (PD):

o Data 0: “Gamma Set (26h)”, Display Command Set (DCS)

o Data 1: 01hex, Parameter of the DCS

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

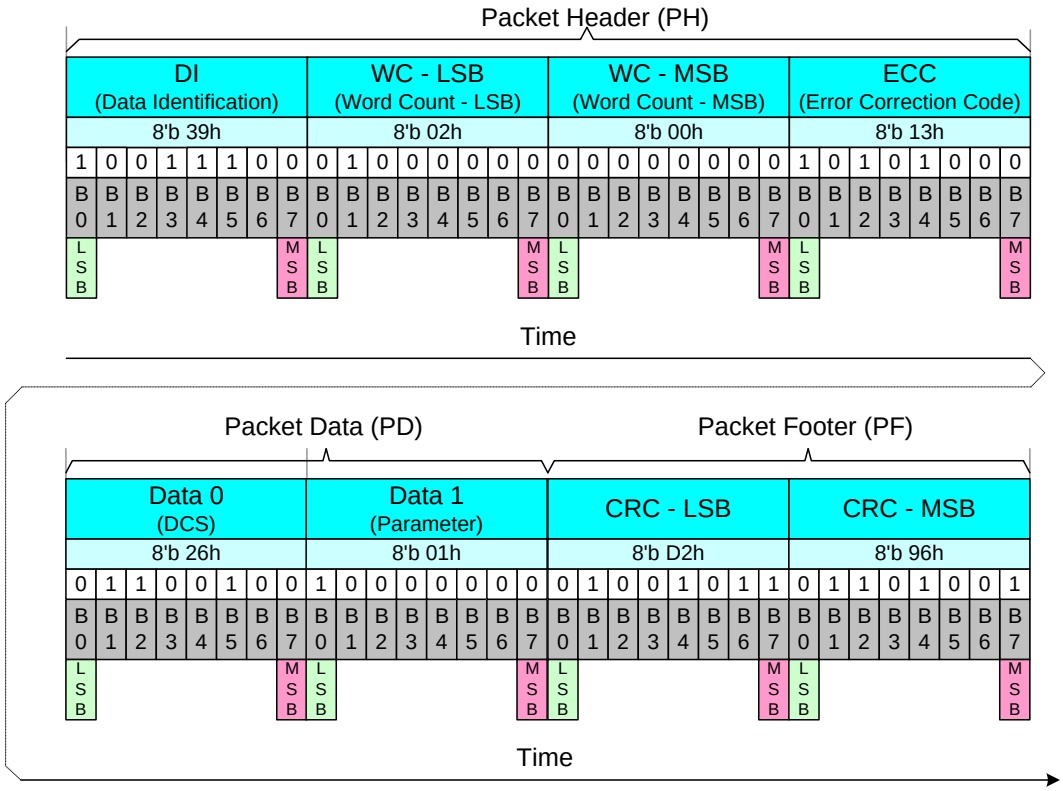


Figure 70 Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

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Long Packet (LPa), when a Write (4 parameters) was sent, is defined e.g.

• Data Identification (DI)

  o Virtual Channel (VC, DI[7…6]): 00b

  o Data Type (DT, DI[5…0]): 11 1001b

• Word Count (WC)

  o Word Count (WC): 0005h

• Error Correction Code (ECC)

• Packet Data (PD):

  o Data 0: “Column Address Set (2Ah)”, Display Command Set (DCS)

  o Data 1: 00hex, 1st Parameter of the DCS, Start Column SC[15…8]

  o Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC[7…0]

  o Data 3: 01hex, 3rd Parameter of the DCS, End Column EC[15…8]

  o Data 4: EFhex, 4th Parameter of the DCS, End Column EC[7…0]

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

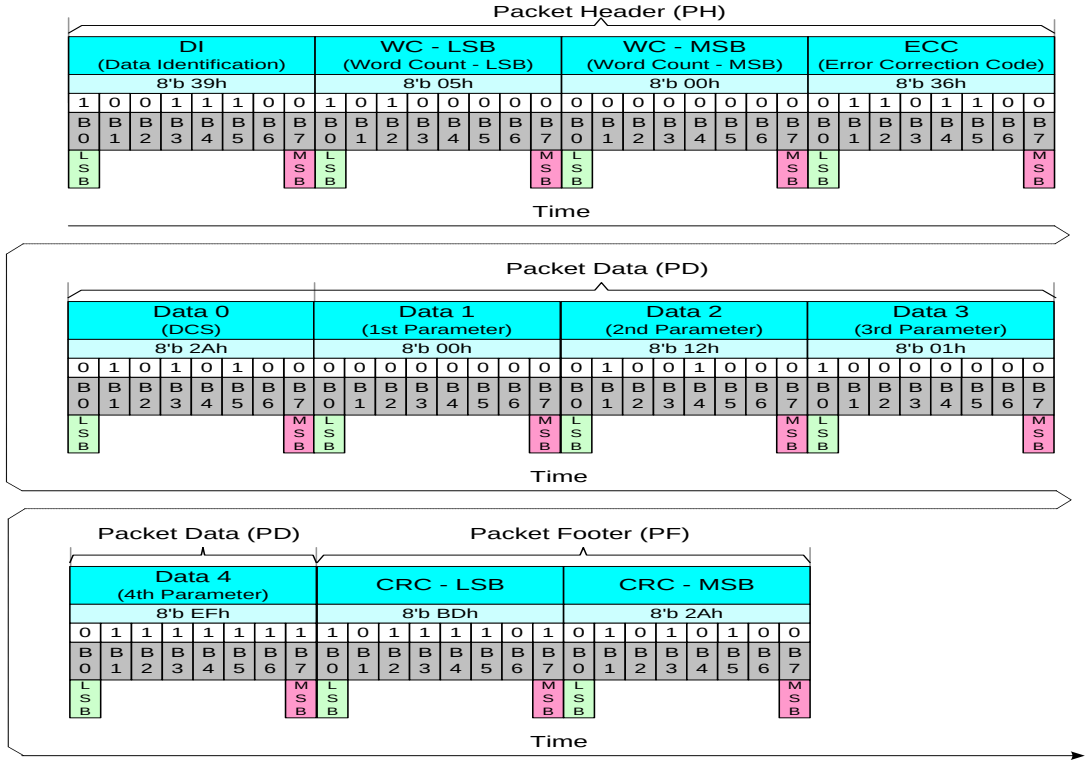


Figure 71 Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

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3.5.39. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MPU to the display module. These commands are defined on a table (See chapter "5.2. Command Description") below.

Table 20 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Page 0 Command
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Content Adaptive Brightness Control (56h)
Read CABC Minimum Brightness (5Fh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

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The MPU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MPU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This same sequence is illustrated for reference purposes below.

Step 1:

• The MPU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module

• Data Identification (DI)

  o Virtual Channel (VC, DI[7…6]): 00b

  o Data Type (DT, DI[5…0]): 11 0111b

• Maximum Return Packet Size (MRPS)

  o Data 0: 01hex

  o Data 1: 00hex

• Error Correction Code (ECC)

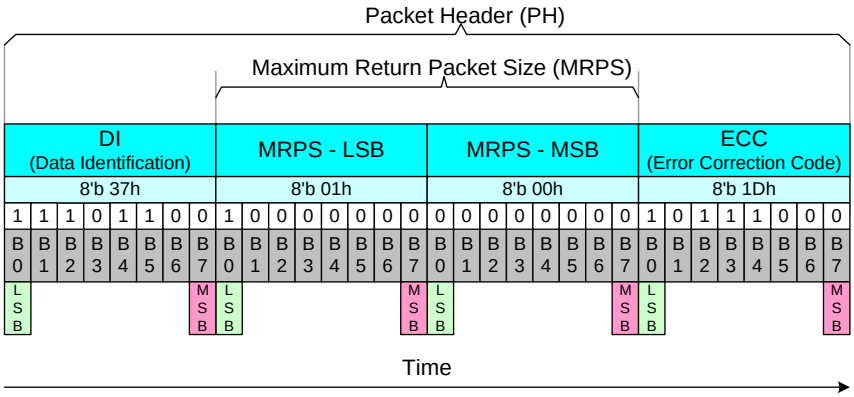


Figure 72 Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

• The MPU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MPU sends “Display Command Set (DCS) Read, No Parameter” to the display module

• Data Identification (DI)

  o Virtual Channel (VC, DI[7…6]): 00b

  o Data Type (DT, DI[5…0]): 00 0110b

• Packet Data (PD)

  o Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)

  o Data 1: Always 00hex

• Error Correction Code (ECC)

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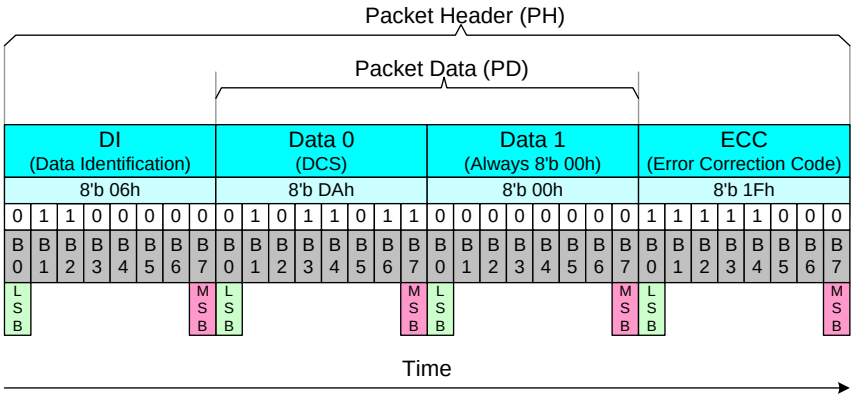


Figure 73 Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MPU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a

   command, See chapter “Acknowledge with Error Report (AwER)”
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

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3.5.40. Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MPU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed.

The display module is ignored Packet Data (PD) what the MPU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

• Data Identification (DI)
  - o Virtual Channel (VC, DI[7…6]): 00b
  - o Data Type (DT, DI[5…0]): 00 1001b

• Word Count (WC)
  - o Word Count (WC): 0005hex

• Error Correction Code (ECC)

• Packet Data (PD):
  - o Data 0: 89hex (Random data)
  - o Data 1: 23hex (Random data)
  - o Data 2: 12hex (Random data)
  - o Data 3: A2hex (Random data)
  - o Data 4: E2hex (Random data)

• Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

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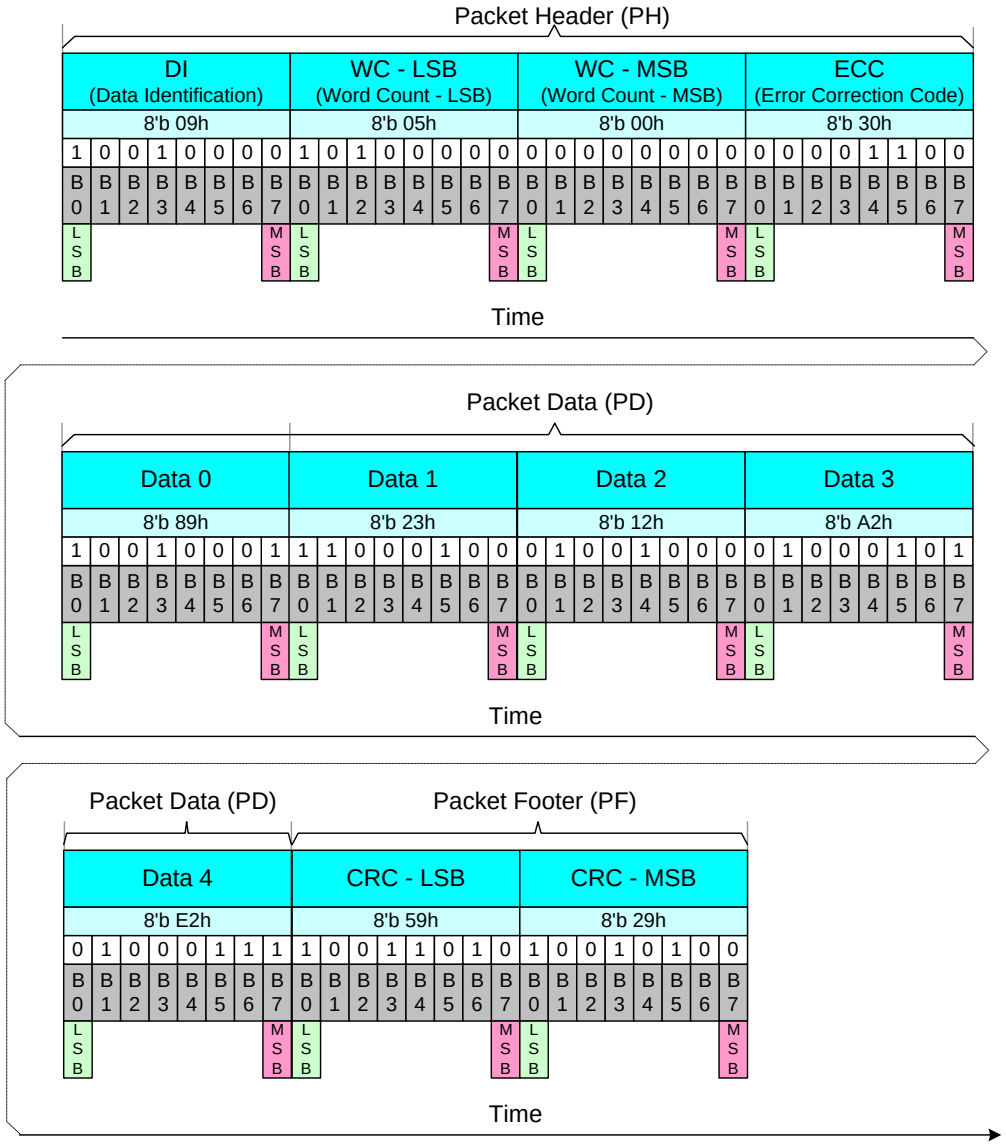


Figure 74 Null Packet, No Data (NP-L) - Example

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3.5.41. End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 1000b), from the MPU to the display module. The purposes of this command is terminated the high Speed Data Transmission (HSDT) mode properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MPU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both: i.e. If the MPU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MPU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= Leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MPU during the Low Power Data Transmission (LPDT) mode.

The summary of the receiving and transmitting EoTP is listed below.

Table 21 Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MPU => Display Module	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Module => MPU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

Short Packet (SPa) is using a fixed format as follows

- Data Identification (DI)
  - o Virtual Channel (VC, DI[7…6]): 00b
  - o Data Type (DT, DI[5…0]): 00 1000b
- Packet Data (PD)
  - o Data 0: 0Fhex
  - o Data 1: 0Fhex
- Error Correction Code (ECC)
  - o ECC: 01hex

This is defined on the Short Packet (SPa) as follows.

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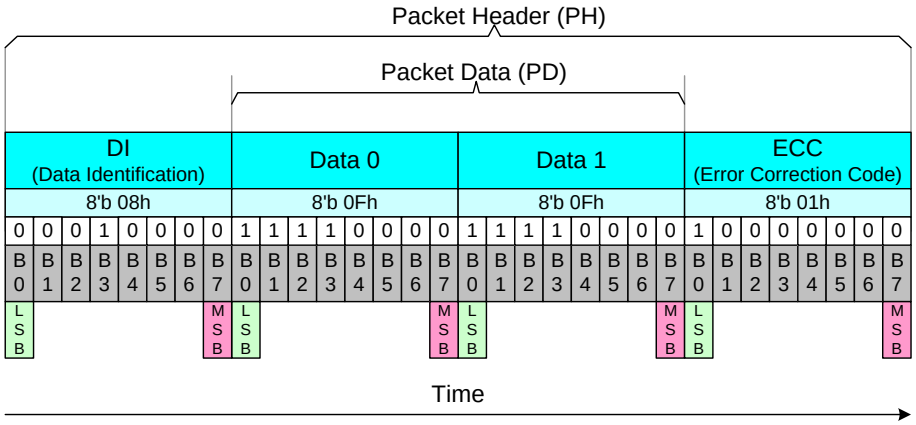


Figure 75 End of Transmission Packet (EoTP)

Some use cases of the “End of Transmission Packet” (EoTP) are illustrated only for reference purposes below.

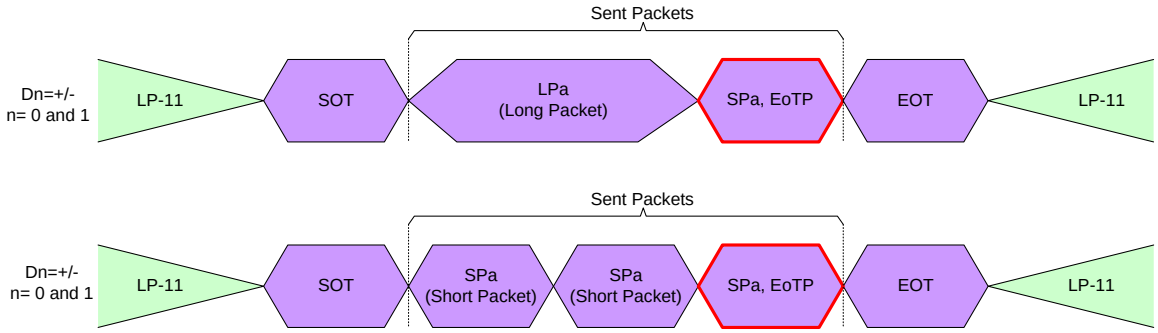


Figure 76 End of Transmission Packet (EoTP)-Examples

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3.5.42. Packet from the Display Module to the MPU

3.5.43. Used Packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MPU after the MPU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “Data Type (DT)”. It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent in one packet.

Both cases are illustrated for reference purposes below.

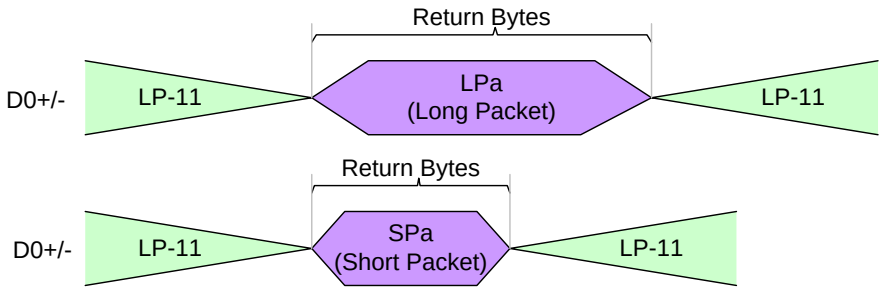


Figure 77 Return Bytes on Single Packet

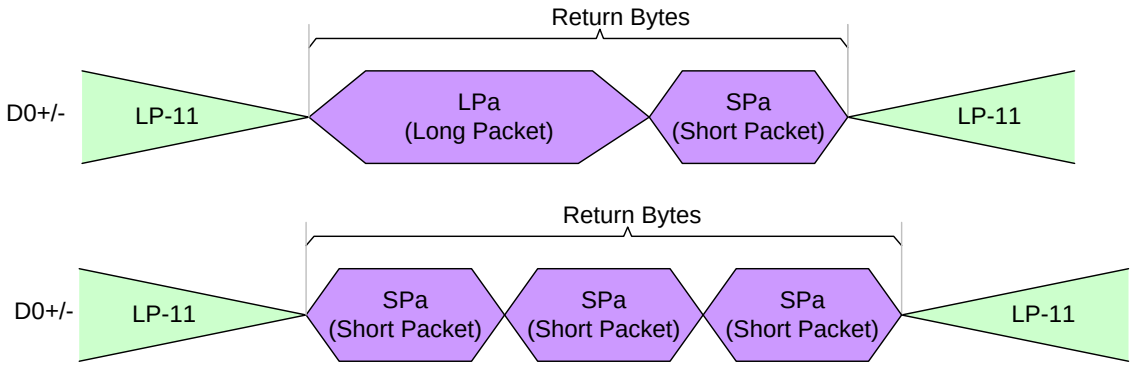


Figure 78 Return Bytes on Several Packets – Not Possible

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Exception:

The display module is returning 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MPU when the display module has received a read command (See chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)”) where has been detected and corrected a single bit error by the EEC (See bit 8 on “Table 22: Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”).

These return packets are illustrated for reference purposes below.

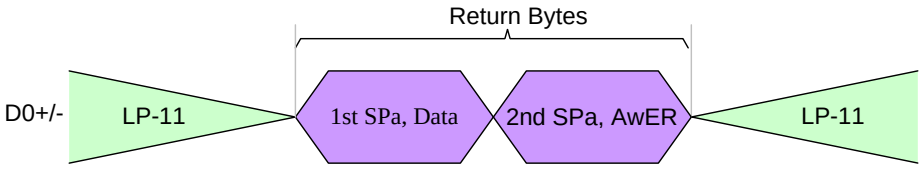


Figure 79 Exception when Return Bytes on Several Packets

AwER = Acknowledge with Error Report

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3.5.44. Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MPU. The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Table 22 Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Table 23 Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Reserved, Set to '0' internally Set to '0' internally (Only for Long Packet (LP)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

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These errors are included from all packages what has been received from the MPU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 00 0010b

• Packet Data (PD)

o Bit 8: ECC Error, single-bit (detected and corrected)

o AwER: 0100h

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

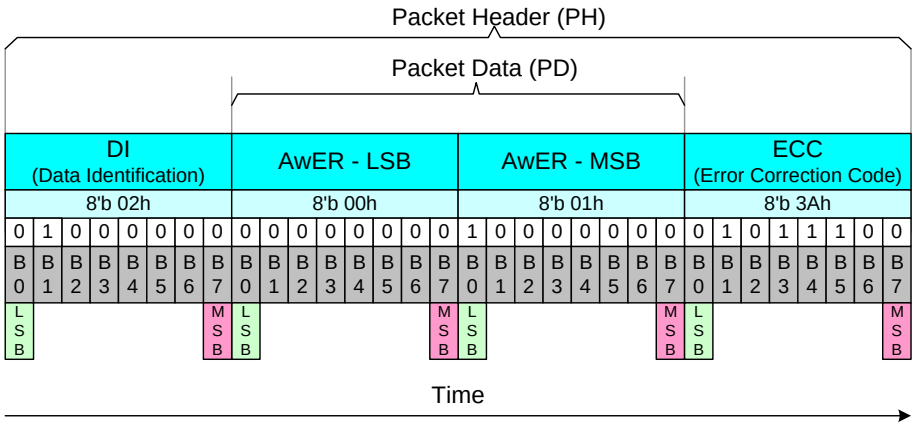


Figure 80 Acknowledge with Error Report (AwER) – Example

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It is possible that the display module has received several packets, which have included errors, from the MPU before the MPU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

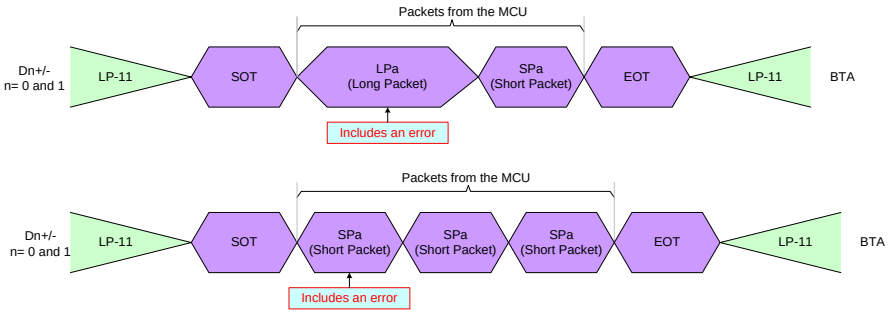


Figure 81 Errors Packets

Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The number of the packets, which are including an ***ECC or CRC*** error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MPU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.

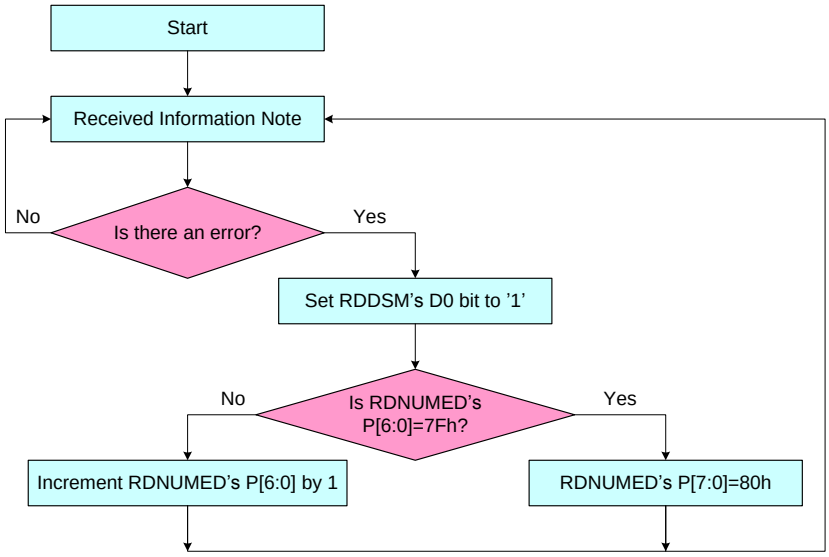


Figure 82 Flow Chart for Errors on DSI[Note]

Note 1. This information can be Interface or Packet Level Communication but it is always from the MPU to the display module in this case.

2. CRC or ECC error

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3.5.45. DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 011100b), from the display module to the MPU.“DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 01 1100b

• Word Count (WC)

o Word Count (WC): 0005hex

• Error Correction Code (ECC)

• Packet Data (PD):

o Data 0: 89hex

o Data 1: 23hex

o Data 2: 12hex

o Data 3: A2hex

o Data 4: E2hex

• Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.

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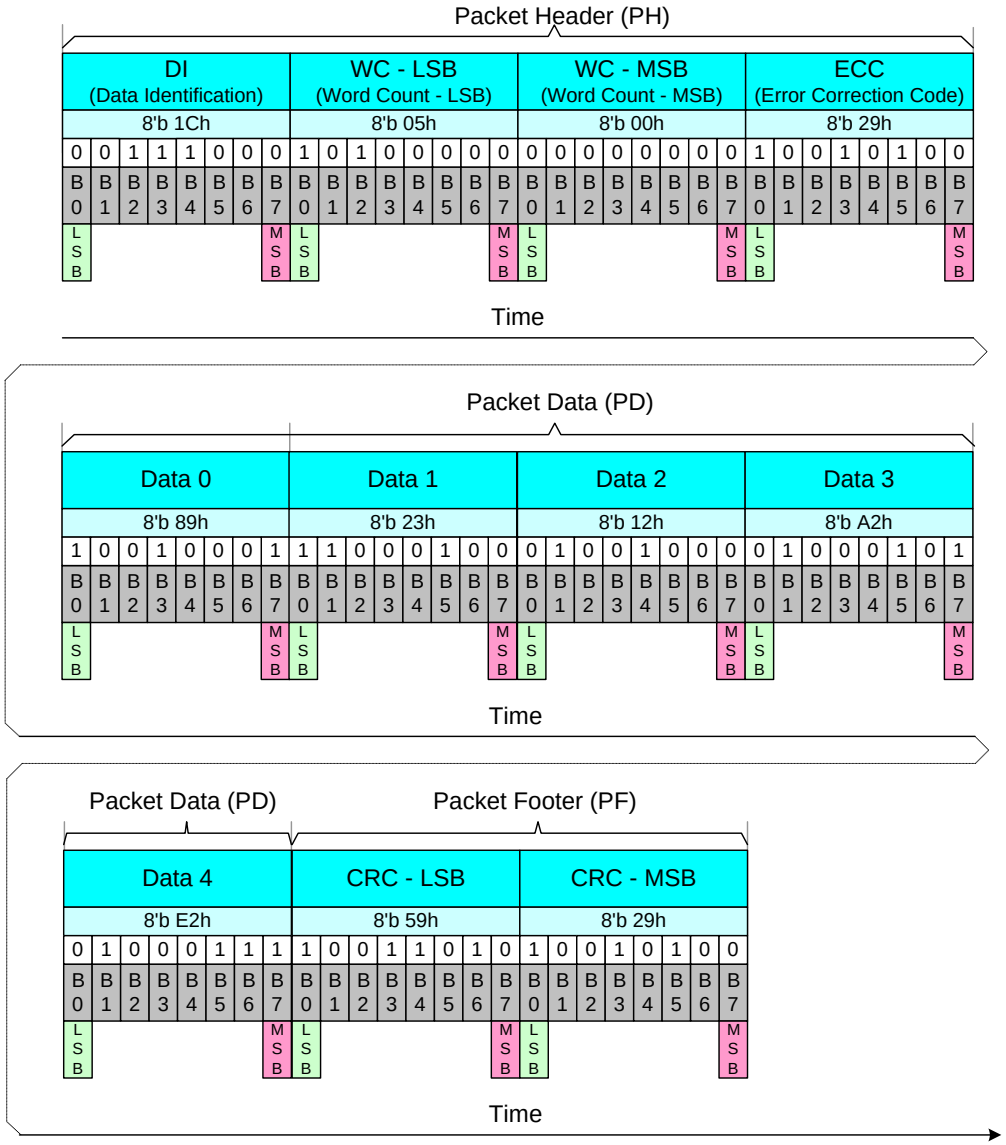


Figure 83 DCS Read Long Response (DCSRR-L) - Example

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3.5.46. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MPU.“DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 10 0001b

• Packet Data (PD)

o Data 0: 45hex

o Data 1: 00hex (Always)

• Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.

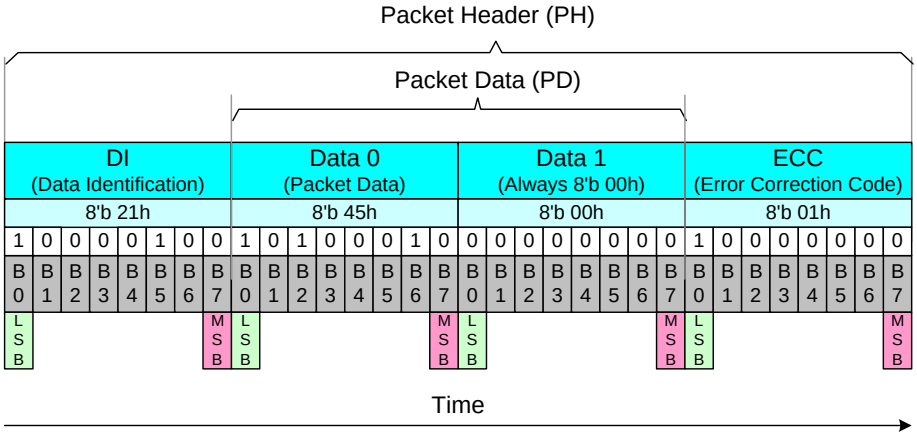


Figure 84 DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

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3.5.47. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MPU.“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MPU has sent to the display module.

Short Packet (SPa) is defined e.g.

• Data Identification (DI)

o Virtual Channel (VC, DI[7…6]): 00b

o Data Type (DT, DI[5…0]): 10 0010b

• Packet Data (PD)

o Data 0: 45hex

o Data 1: 32hex

• Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

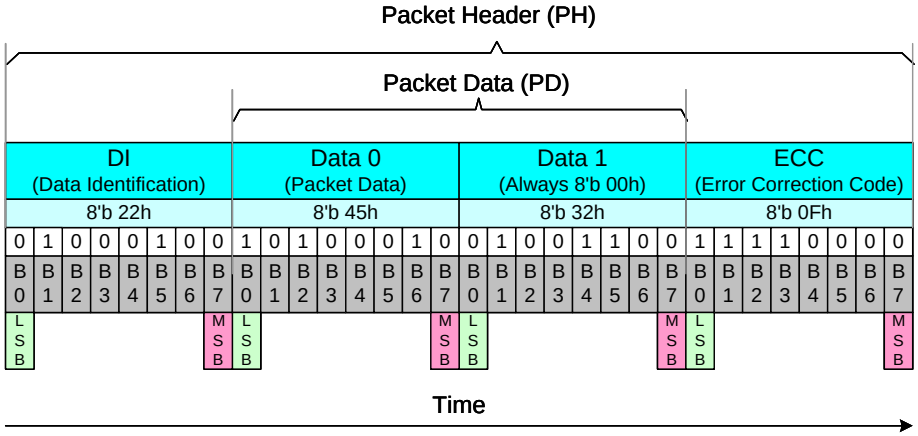


Figure 85 DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

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3.5.48. Communication Sequences

3.5.49. General

The communication sequences can be done on interface or packet levels between the MPU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes (DSI-D0+/- and DSI-D1+/-) and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically. See chapter “DSI-CLK Lanes”.

Functions of the interface level communication is described on the following table.

Table 24 Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described on the following table.

Table 25 Packet Level Communication

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MPU	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW-L	Long Packet	DCS Write Long
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data
	EoTP	Short Packet	End of Transmission Packet
Display Module (ILI9806E-2C)	AwER	Short Packet	Acknowledge with Error Packet
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response
	DCSRR2-S	Short Packet	DCS Read Short Response

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3.5.50. Sequences

3.5.51. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used, is described on following tables.

Table 26 DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSW1-S	LPDT	➔	--	--	
3	--	LP-11	➔	--	--	End

Table 27 DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSW1-S	HSDT	➔	--	--	
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	End

Table 28 DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	DCSW1-S	HSDT	➔	--	--	
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	➔	LP-11	--	If No Error ➔ Go to Line 8 If Error Occurs ➔ Go to Line 13
7						
8	--	--	➔	ACK	--	No Error
9	--	--	➔	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	➔	--	--	End
12						
13	--	--	➔	LPDT	AwER	Error Report
14	--	--	➔	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	➔	--	--	End

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3.5.52. DCS Write, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" is defined on chapter "Display Command Set (DCS) Write, No Parameter (DCSWN-S)" and example sequences, how this packet is used, is described on following tables.

Table 29 DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 30 DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 31 DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

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3.5.53. DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

Table 32 DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 33 DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 34 DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSRN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

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3.5.54. DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

Table 35 DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
23	--	LP-11	→	--	--	End

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Table 36 DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	SMRPS-S	HSDT	➔	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	➔	--	--	Wanted to get a response ID1(DAh)
4	EoTP	HSDT	➔	--	--	End of Transmission Packet
5	--	LP-11	➔	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MPU to the display module
7	--	--	➔	LP-11	--	If No Error ➔ Go to Line 9 If Error Occurs ➔ Go to Line 14 If Error is Corrected by ECC ➔ Go to Line 19
8						
9	--	--	➔	LPDT	DCSRR-L	Response 200 byte return
10	--	--	➔	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
12	--	LP-11	➔	--	--	End
13						
14	--	--	➔	LPDT	AwER	Error Report
15	--	--	➔	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
17	--	LP-11	➔	--	--	End
18						
19	--	--	➔	LPDT	DCSRR-S	Response 200 byte return
20	--	--	➔	LPDT	AwER	Error Report (Error is corrected by ECC)
21			➔	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MPU
23	--	LP-11	➔	--	--	End

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3.5.55. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and an example sequence, how this packet is used, is described on the following table.

Table 37 Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	NP-L	HSDT	➔	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	End

3.5.56. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined on chapter “8.1.3.2.1.7 End of Transmission Packet (EoTP)” and an example sequence, how this packet is used, is described on the following table.

Table 38 End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MPU		Information Direction	Display Module (**ILI9806E-2C**)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	NP-L	HSDT	➔	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	End

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3.6. Display Data Format

3.6.1. DPI (RGB) Interface

3.6.2. 16-bit / pixel 65K colors order on the DPI Interface

The 16-bit RGB interface is selected by setting the DPI[2:0] bits to “101”. The display operation is synchronized with VS, HS and PCLK signals.

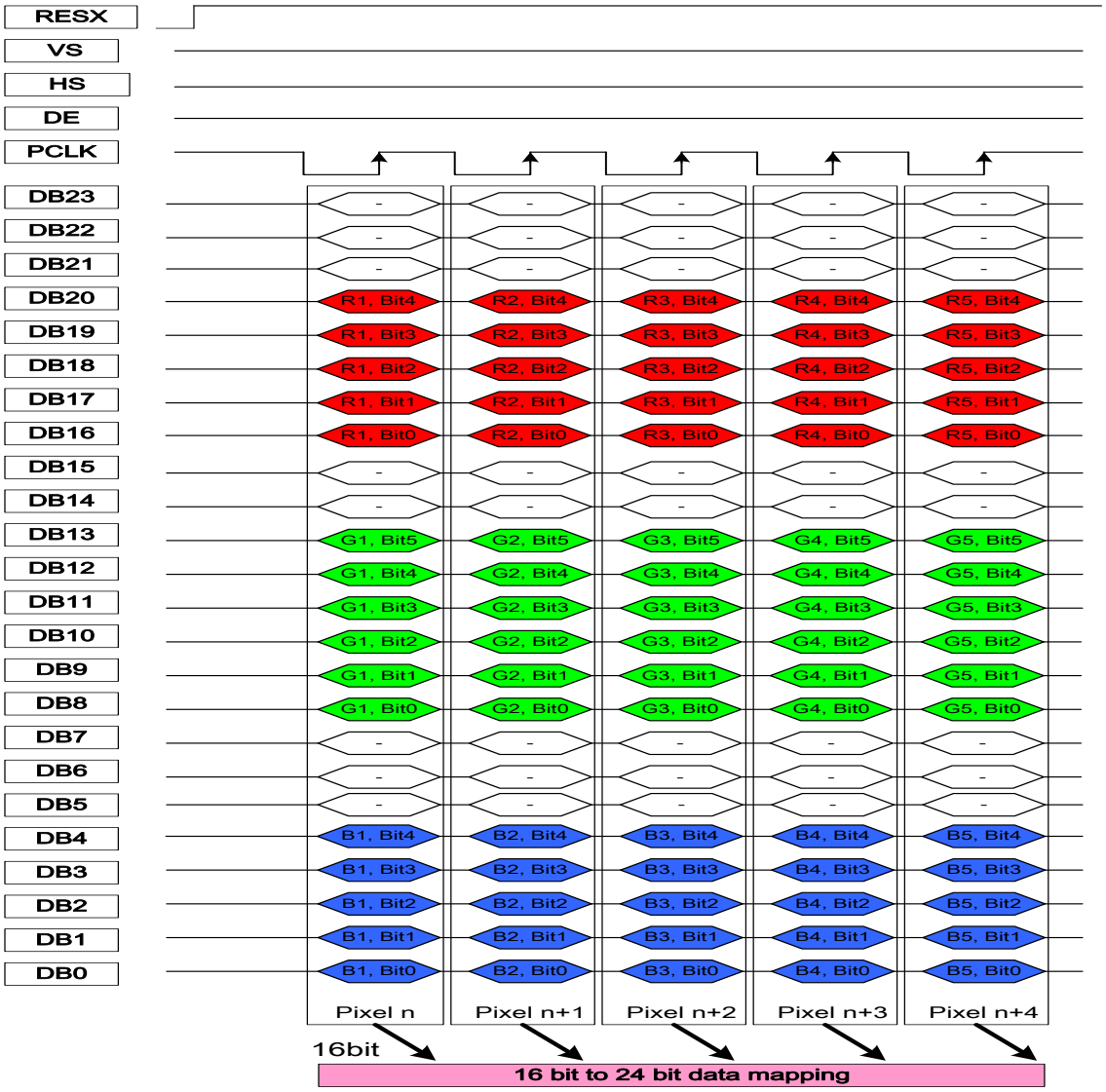


Figure 86 16-bit / pixel 65K colors order on the DPI Interface

Note:

1. The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, MSB=Bit 4, LSB=Bit 0 for Red and Blue data.
2. 1-times transfer is used to transmit 1 pixel data to the 16-bit color depth information.
3. ‘-‘= void

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3.6.3. 18-bit / pixel 262K colors order on the DPI Interface

The 18-bit RGB interface is selected by setting the DPI[2:0] bits to “110”. The display operation is synchronized with VS, HS and PCLK signals.

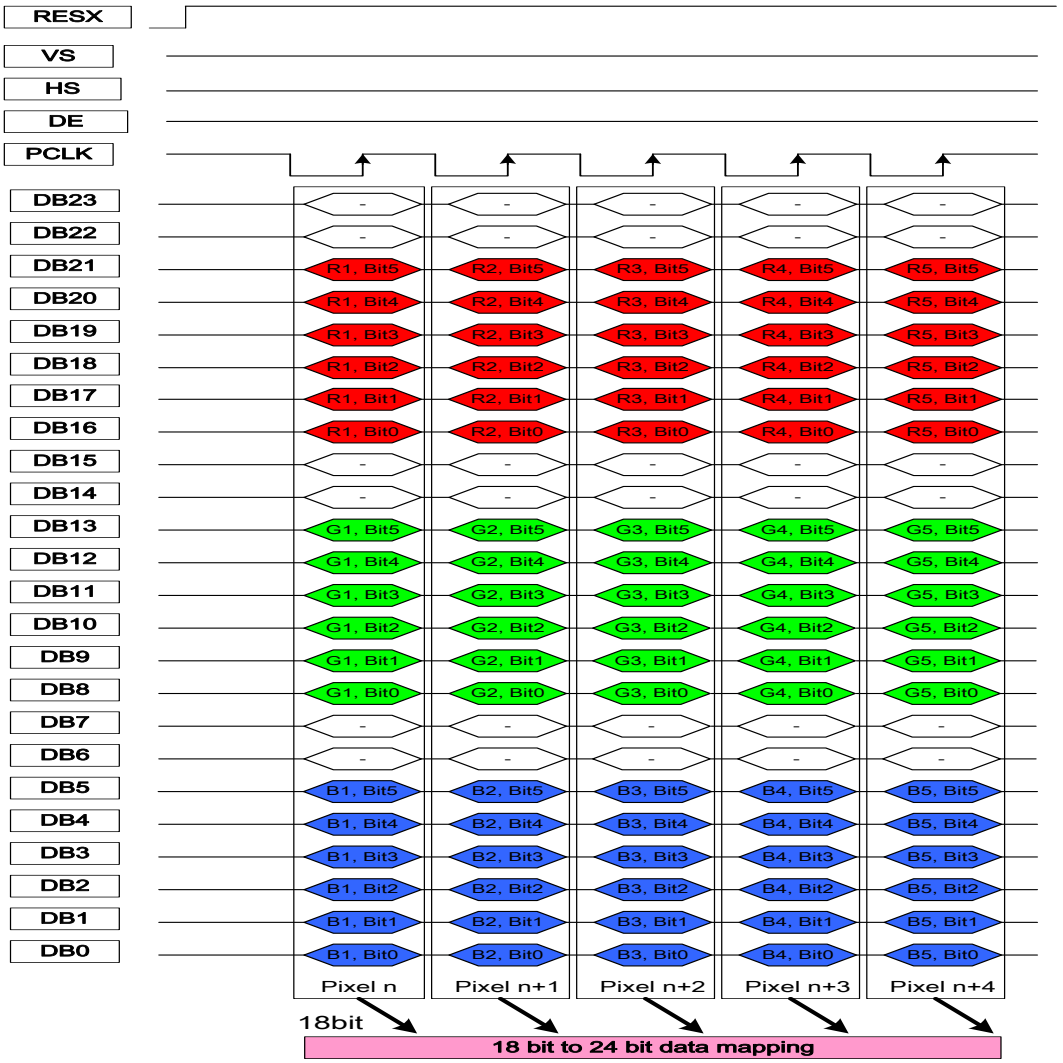


Figure 87 18-bit / pixel 262K colors order on the DPI Interface

Note:

1. The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, Red and Blue data.
2. 1-times transfer is used to transmit 1 pixel data to the 18-bit color depth information.
3. ‘-‘= void

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3.6.4. 24-bit / pixel 16.7M colors order on the DPI Interface

The 24-bit RGB interface is selected by setting the DPI[2:0] bits to “111”. The display operation is synchronized with VS, HS and PCLK signals.

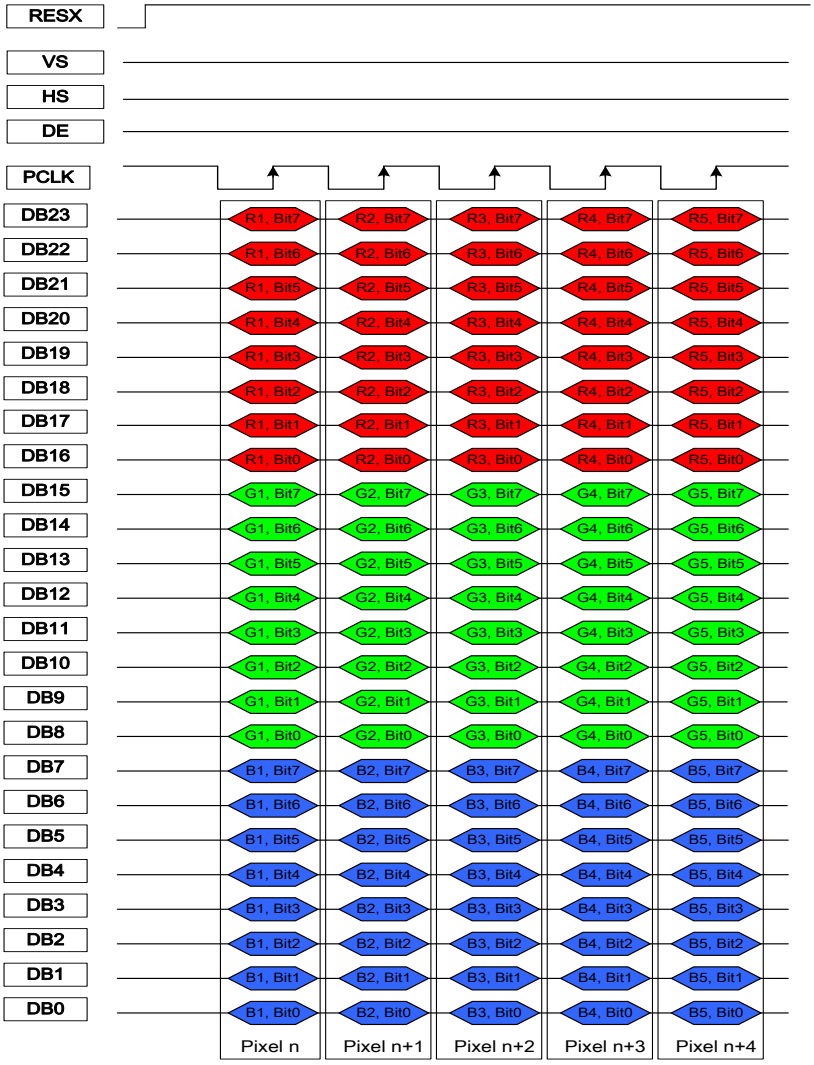


Figure 88 24-bit / pixel 16.7M colors order on the DPI Interface

Note:

1. The data order is as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit 7, LSB=Bit 0 for Green, Red and Blue data.
2. 1-times transfer is used to transmit 1 pixel data to the 24-bit color depth information.

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3.6.5. DSI transmission data format

3.6.6. 16-bit per Pixel, Long packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, ILI9806E-2C has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifice.

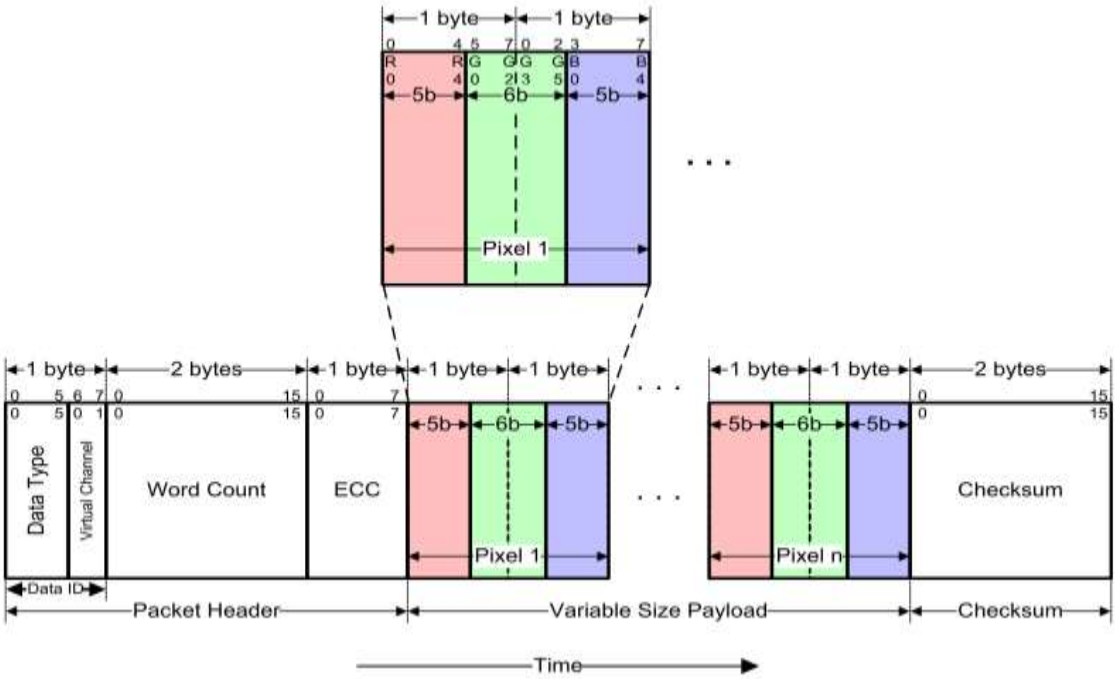


Figure 89 16-bit per Pixel, Data Type 00 1110 (0Eh)

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3.6.7. 18-bit per Pixel, Long packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four 1246 pixels (nine bytes).

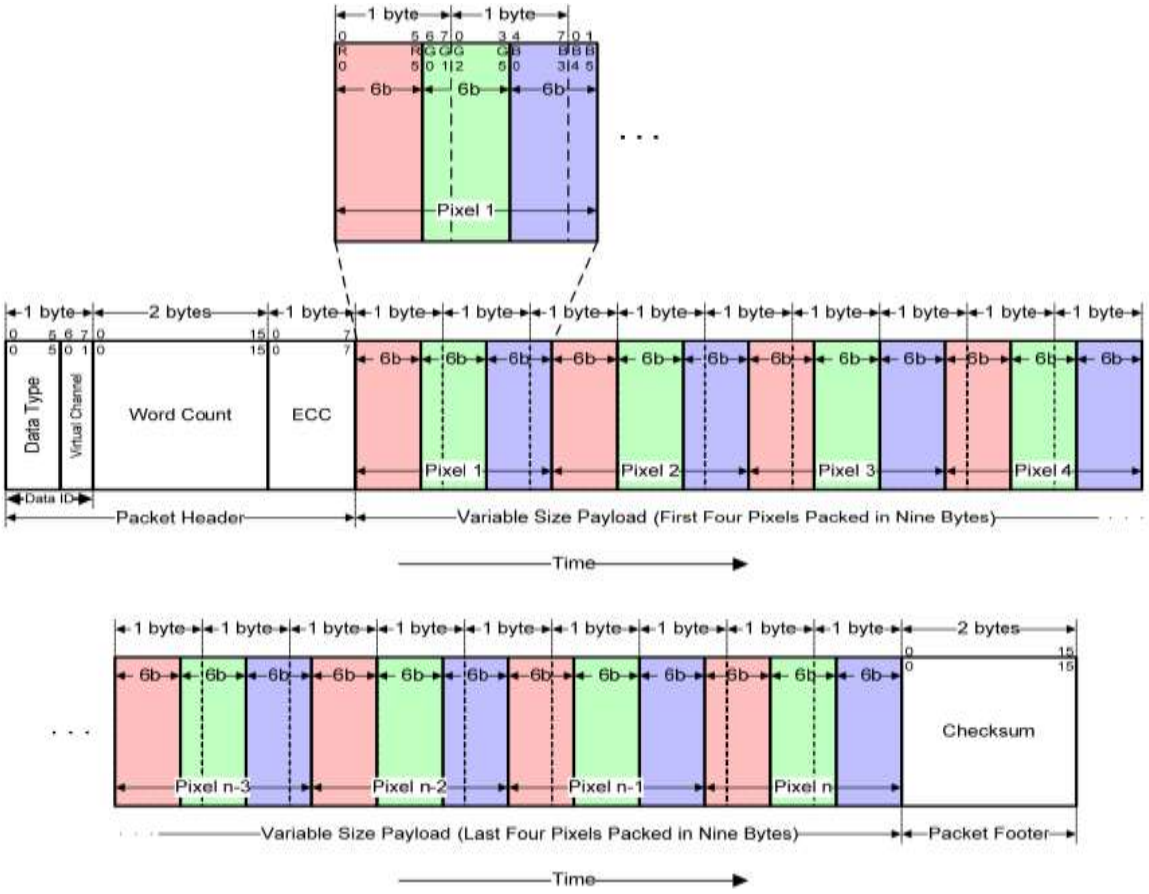


Figure 90 18-bit per Pixel, Data Type = 01 1110 (1Eh)

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3.6.8. 18-bit per Pixel, Long packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

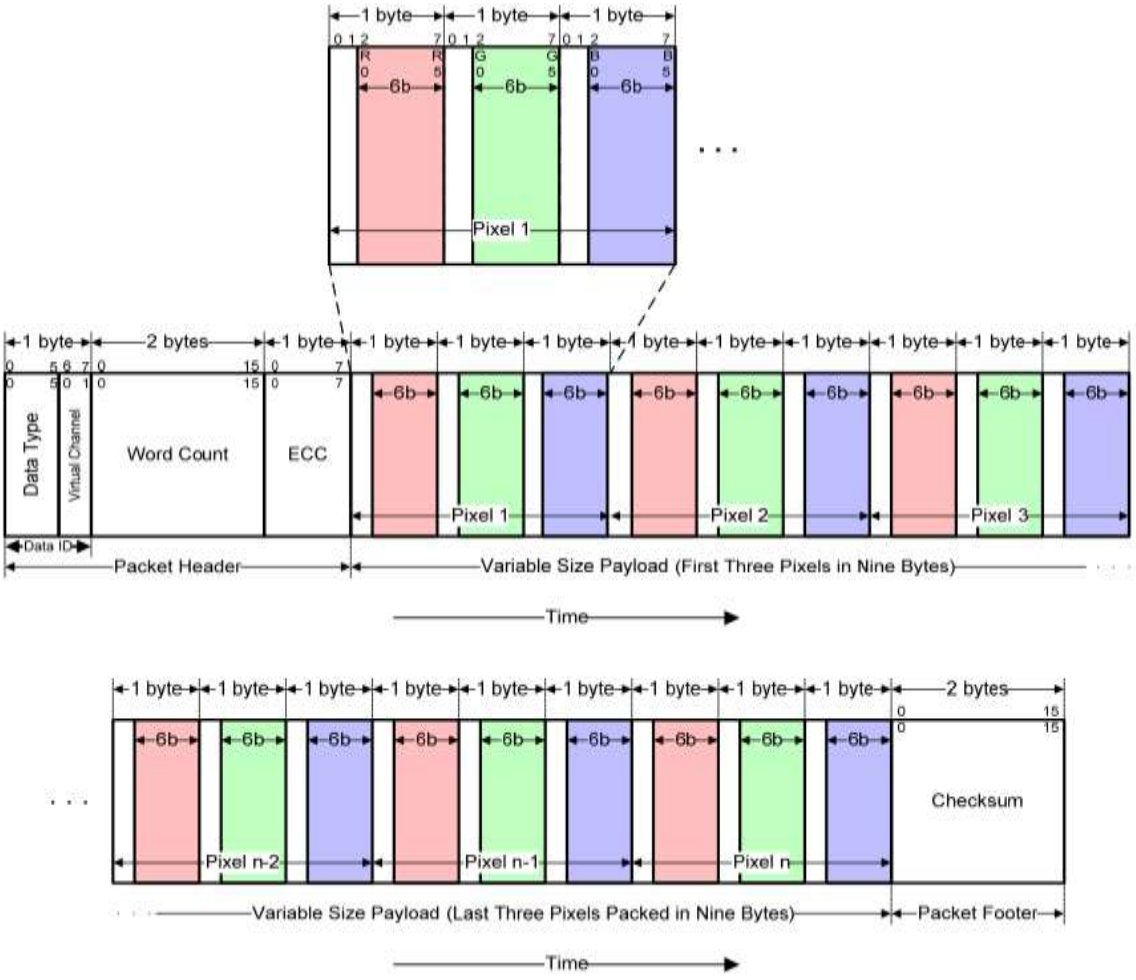


Figure 91 18-bit per Pixel, Data Type = 10 1110 (2Eh)

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3.6.9. 24-bit per Pixel, Long packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

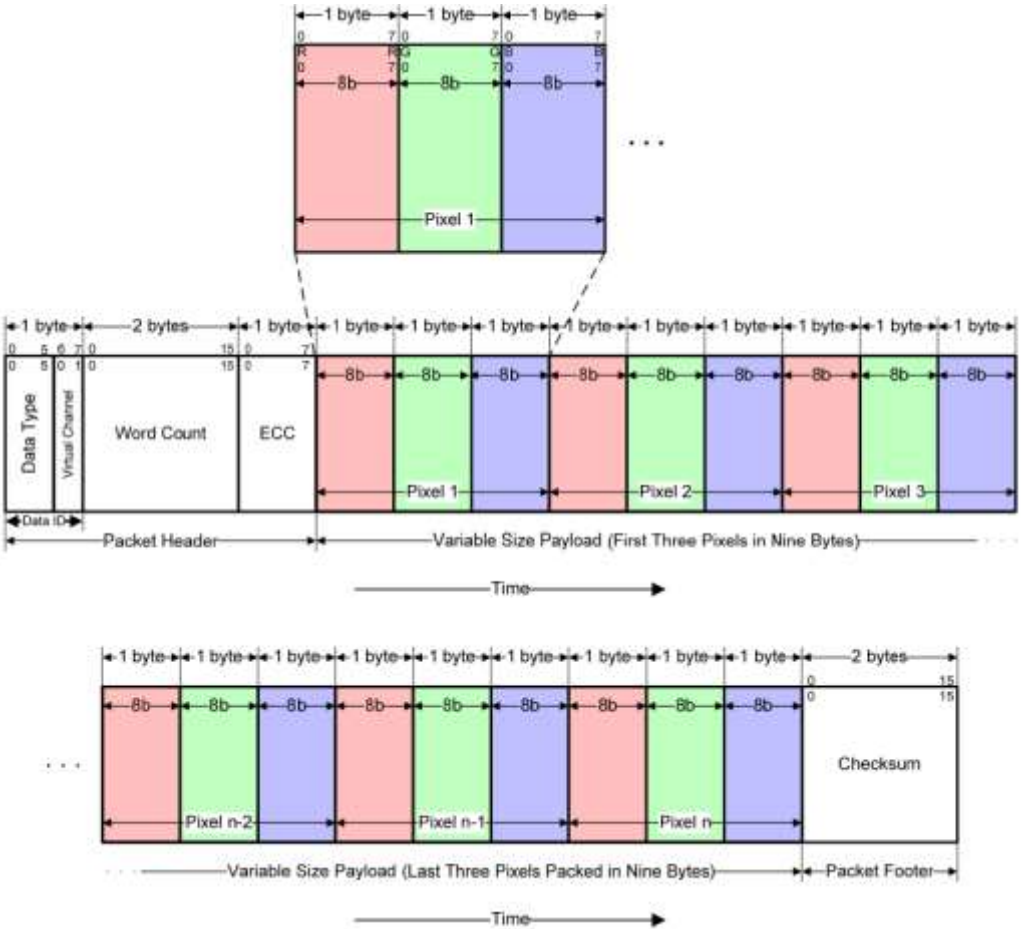


Figure 92 24-bit per Pixel, Data Type = 11 1110 (3Eh)

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4. Command

4.1. Command Flow

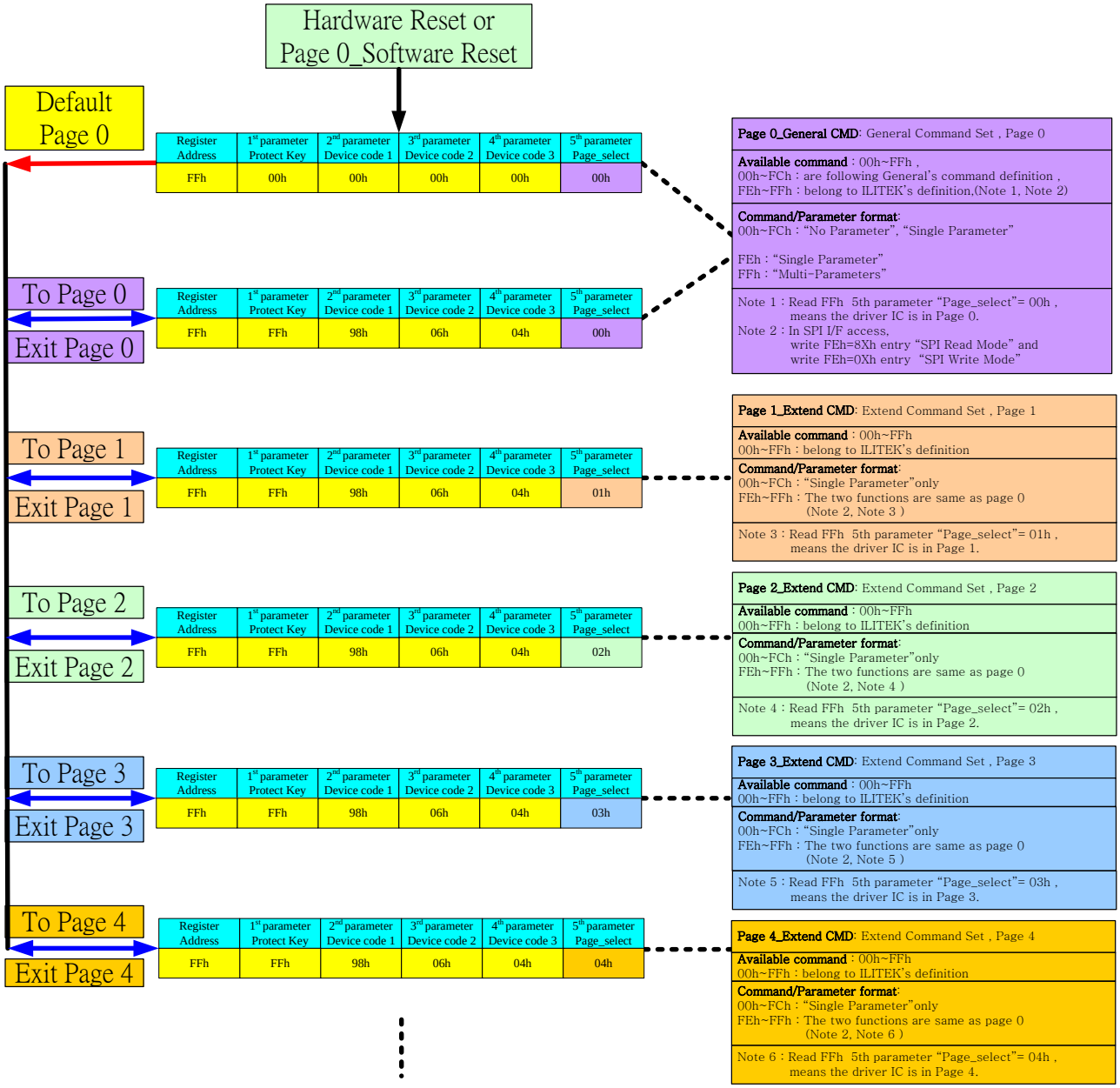


Figure 93 Command Flow

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4.2. Command List

4.2.1. Page 0 Command List

Page 0 Command Set		00h : NOP (No Operation)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h

Page 0 Command Set		01h : SWRESET (Software Reset)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	1	01h

Page 0 Command Set		05h : RDNUMED (Read Number of the Errors on DSI)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	1	05h
1st Parameter	Read	P [7:0]								XXh

Page 0 Command Set		0Ah : RDDPM (Read Display Power Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Read	BSTON	0	0	SLPOUT	NORON	DISON	0	0	XXh

Page 0 Command Set		0Bh : RDDMADCTL (Read Display MADCTL)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	1	0Bh
1st Parameter	Read	0	0	0	0	BGR	0	SS	GS	XXh

Page 0 Command Set		0Ch : RDDCOLMOD (Read Display COLMOD)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	0	0	0Ch
1st Parameter	Read	0	DPI [2:0]			0	0	0	0	XXh

Page 0 Command Set		0Dh : RDDIM (Read Display Image Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	0	1	0Dh
1st Parameter	Read	0	0	INVON	ALLPON	ALLPOFF	GCS [2:0]			XXh

Page 0 Command Set		0Eh : RDDSM (Read Display Signal Mode)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	1	0	0Eh
1st Parameter	Read	TEON	0	HSON	VSON	PCLKON	DEON	0	EODSI	XXh

Page 0 Command Set		0Fh : RDDSDR (Read Display Self-Diagnostic Result)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	1	1	0Fh
1st Parameter	Read	REGLD	FUNDT	0	0	0	0	0	0	XXh

Page 0 Command Set		10h : SLPIN (Sleep In)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	0	10h

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Page 0 Command Set		11h : SLPOUT (Sleep Out)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	1	11h

Page 0 Command Set		13h : NORON (Normal Display Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	1	1	13h

Page 0 Command Set		20h : INVOFF (Display Inversion Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	20h

Page 0 Command Set		21h : INVON (Display Inversion ON)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	1	21h

Page 0 Command Set		22h : ALLPOFF (All pixels off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	0	22h

Page 0 Command Set		23h : ALLPON (All pixels on)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	1	23h

Page 0 Command Set		26h : GAMSET (Gamma Set)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	1	0	26h
1st Parameter	Write	GC[7:0]								01h

Page 0 Command Set		28h : DISPOFF (Display Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	0	28h

Page 0 Command Set		29h : DISPON (Display ON)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	1	29h

Page 0 Command Set		34h : TEOFF (Tearing Effect Line OFF)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	0	34h

Page 0 Command Set		35h : TEON (Tearing Effect Line ON)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	1	35h

Page 0 Command Set		36h : MADCTL (Display Access Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	1	0	36h
1st Parameter	Write	0	0	0	0	BGR	0	SS	GS	xx

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Page 0 Command Set		3Ah : COLMOD (Interface Pixel Format)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	1	0	1	0	3Ah
1st Parameter	Write	0	DPI[2:0]			0	0	0	0	70h

Page 0 Command Set		51h : WRDISBV (Write Display Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	0	1	51h
1st Parameter	Write	DBV[7:0]								xx

Page 0 Command Set		52h : RDDISBV (Read Display Brightness Value)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	0	52h
1st Parameter	Read	DBV[7:0]								xx

Page 0 Command Set		53h : WRCTRLD (Write Control Display)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write	0	0	BCTRL	0	DD	BL	0	0	xx

Page 0 Command Set		54h : RDCTRLD (Read Control Display Value)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	0	54h
1st Parameter	Read	0	0	BCTRL	0	DD	BL	0	0	xx

Page 0 Command Set		55h : WRCABC (Write Content Adaptive Brightness Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	1	55h
1st Parameter	Write	C[7:4]				C[3:0]				xx

Page 0 Command Set		56h : RDCABC (Read Content Adaptive Brightness Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	1	0	56h
1st Parameter	Read	C[7:4]				C[3:0]				xx

Page 0 Command Set		5Eh : WRCABCMB (Write CABC Minimum Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	1	1	0	5Eh
1st Parameter	Write	CMB[7:0]								xx

Page 0 Command Set		5Fh : RDCABCMB (Read CABC Minimum Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	1	1	1	5Fh
1st Parameter	Read	CMB[7:0]								xx

Page 0 Command Set		68h : RDABCSDR (Read automatic brightness control self-diagnostic result)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	1	0	0	0	68h
1st Parameter	Read	D[7:6]		0	0	0	0	0	0	xx

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Page 0 Command Set		DAh : RDID1 (Read ID1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	0	DAh
1st Parameter	Read	ID1[7:0]								xx

Page 0 Command Set		DBh : RDID2 (Read ID2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	1	DBh
1st Parameter	Read	ID2[7:0]								xx

Page 0 Command Set		DCh : RDID3 (Read ID3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	1	0	0	DCh
1st Parameter	Read	ID3[7:0]								xx

Page 0 Command Set		FEh : RDEXTCSPI(Read EXTC command In SPI)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	1	1	1	1	0	FEh
1st Parameter	Write	EXT_SPI_R_EN	EXT_SPI_CNT[6:0]							00h

Page 0 Command Set		FFh : ENEXTC (EXTC command set enable register)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	1	1	1	1	1	FFh
1st Parameter	Write	1	1	1	1	1	1	1	1	FFh
2nd Parameter	Write	1	0	0	1	1	0	0	0	98h
3rd Parameter	Write	0	0	0	0	0	1	1	0	06h
4th Parameter	Write	0	0	0	0	0	1	0	0	04h
5th Parameter	Write / Read	PAGE[7:0]								00h

Note:

1. Undefined commands are treated as NOP (00h) command.

2. FEh to FFh are display supplier for usage of factory .

3. Commands 10h, 13h, 26h, 28h, 29h, 36h (only Bit D4) are updated during V-SYNC,when module is in Sleep Out mode ,to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep In mode and Sleep Out mode.

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4.2.2. Page 1 Command List

Page 1 Command Set		00h : RDID4 (Read ID 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	Read	ID4[23:16]								98h

Page 1 Command Set		01h : RDID4 (Read ID 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	1	01h
1st Parameter	Read	ID4[15:8]								06h

Page 1 Command Set		02h : RDID4 (Read ID 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	0	02h
1st Parameter	Read	ID4[7:0]								04h

Page 1 Command Set		08h : IFMODE.1 (Interface Mode Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	0	0	08h
1st Parameter	Write / Read	0	0	0	SDO_STATUS	SEPT_SDIO	0	0	0	08h

Page 1 Command Set		0Ah : IFMODE 2 (Interface Mode Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Write / Read	0	0	0	0	0	0	0	2LANE_En	00h

Page 1 Command Set		20h : DISCTRL1 (Display Function Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	20H
1st Parameter	Write / Read	0	0	0	0	0	0	0	SYNC MODE	00h

Page 1 Command Set		21h : DISCTRL2 (Display Function Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	1	21h
1st Parameter	Write / Read	0	0	0	0	VSPL	HSPL	DPL	EPL	01h

Page 1 Command Set		22h : PANELCTRL1 (Set panel operation mode1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	0	22h
1st Parameter	Write / Read	0	0	0	0	BGR_PANEL	0	SS_PANEL	GS_PANEL	00h

Page 1 Command Set		23h : PANELCTRL2 (Set panel operation mode2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	1	23h
1st Parameter	Write / Read	0	0	0	0	0	0	REV	0	00h

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Page 1 Command Set		24h : Data Complement Setting								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	0	0	24h
1st Parameter	Write / Read	0	0	0	0	0	0	EPF[1:0]		03h

Page 1 Command Set		25h : BLKPRH 1 (Blanking Porch 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	0	1	25H
1st Parameter	Write / Read	0	VFP[6:0]							14h

Page 1 Command Set		26h : BLKPRH 2 (Blanking Porch 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	1	0	26H
1st Parameter	Write / Read	0	VBP[6:0]							14h

Page 1 Command Set		27h : BLKPRH 3 (Blanking Porch 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	1	1	27H
1st Parameter	Write / Read	HBP[7:0]								05h

Page 1 Command Set		28h : BLKPRH 4 (Blanking Porch 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	0	28H
1st Parameter	Write / Read	0	0	0	0	0	0	HBP[9:8]		00h

Page 1 Command Set		30h : RESCTRL (Resolution Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	0	0	0	30h
1st Parameter	Write / Read	0	0	0	0	0	RES[2:0]			02h

Page 1 Command Set		31h : INVTR (Display Inversion Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	0	0	1	31H
1st Parameter	Write / Read	0	0	0	0	NLA[3:0]				00h

Page 1 Command Set		34h : DITHE (Dithering Enable)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	0	34h
1st Parameter	Write / Read	0	0	0	0	0	0	0	DITH_EN	00h

Page 1 Command Set		35h : Source Signal Adjust								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	1	35h
1st Parameter	Write / Read	0	0	0	0	0	CHOPPER SEL_REG[2:0]			06h

Page 1 Command Set		40h : PWCTRL 1 (Power Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	0	0	40h
1st Parameter	Write / Read	EXB1T	0	EXT_CPCK_SEL[1:0]		BT [3:0]				15h

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Page 1 Command Set		41h : PWCTRL 2 (Power Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	0	1	41h
1st Parameter	Write / Read	0	DDVDH_CLP[2:0]			0	DDVDL_CLP[2:0]			22h

Page 1 Command Set		42h : PWCTRL 3 (Power Control 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	1	0	42h
1st Parameter	Write / Read	0	0	VGH_CP[1:0]		0	0	VGL_CP[1:0]		02h

Page 1 Command Set		43h : PWCTRL 4 (Power Control 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	1	1	43h
1st Parameter	Write / Read	VGH_CLP EN	0	0	0	VGH_CLP[3:0]				09h

Page 1 Command Set		44h : PWCTRL 5 (Power Control 5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	0	0	44h
1st Parameter	Write / Read	VGL_CLP EN	0	0	0	VGL_CLP[3:0]				86h

Page 1 Command Set		45h : PWCTRL 6 (Power Control 6)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	0	1	45h
1st Parameter	Write / Read	VGH_REG[3:0]				VGL_REG[3:0]				00h

Page 1 Command Set		46h : PWCTRL 7 (Power Control 7)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	1	0	46h
1st Parameter	Write / Read	0	DDVDH_PK1[2:0]			0	DDVDL_PK2[2:0]			33h

Page 1 Command Set		47h : PWCTRL 8 (Power Control 8)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	1	1	47h
1st Parameter	Write / Read	0	VCL_PK3[2:0]			0	VGHL_PK4[2:0]			33h

Page 1 Command Set		50h : PWCTRL 9 (Power Control 9)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	0	0	50h
1st Parameter	Write / Read	VREG1[7:0]								78h

Page 1 Command Set		51h : PWCTRL 10 (Power Control 10)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	0	1	51h
1st Parameter	Write / Read	VREG2[7:0]								78h

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Page 1 Command Set		52h : VMCTRL1 (VCOM Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	0	52h
1st Parameter	Write / Read	0	0	0	0	0	0	0	VCM1[8]	00h

Page 1 Command Set		53h : VMCTRL2 (VCOM Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write / Read	VCM1[7:0]								6Fh

Page 1 Command Set		54h : VMCTRL3 (VCOM Control 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	0	54h
1st Parameter	Write / Read	0	0	0	0	0	0	0	VCM2[8]	00h

Page 1 Command Set		55h : VMCTRL4 (VCOM Control 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	1	55h
1st Parameter	Write / Read	VCM2[7:0]								6Fh

Page 1 Command Set		56h : VMCTRL5 (VCOM Control 5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	1	0	56h
1st Parameter	Write / Read	0	0	0	NVM2	0	0	0	NVM1	00h

Page 1 Command Set		57h : LVD (Low Voltage Detection)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	1	1	57h
1st Parameter	Write / Read	0	VDET[2:0]			0	VCORE_VD[2:0]			20h

Page 1 Command Set		58h : ETMOD (Entry Mode Set)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	0	0	0	58h
1st Parameter	Write / Read	LVD	0	0	1	0	0	0	DSTB	90h

Page 1 Command Set		60h : Source Timing Adjust 1								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	0	0	60h
1st Parameter	Write / Read	0	0	SDTI[5:0]						05h

Page 1 Command Set		61h : Source Timing Adjust 2								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	0	1	61h
1st Parameter	Write / Read	0	0	CRTI[5:0]						05h

Page 1 Command Set		62h : Source Timing Adjust 3								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	1	0	62h
1st Parameter	Write / Read	0	0	EQTI[5:0]						0Eh

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Page 1 Command Set		63h : Source Timing Adjust 4								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	1	1	63h
1st Parameter	Write / Read	0	0	PCTI[5:0]						05h

Page 1 Command Set		80h : Synchronization Timing Adjust 1								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	0	0	0	0	0	80h
1st Parameter	Write / Read	TOUCH_OPT[1:0]		VSOD[1:0]		HOSM[1:0]		HS_OPT	0	00h

Page 1 Command Set		81h : Synchronization Timing Adjust 2								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	0	0	0	0	1	81h
1st Parameter	Write / Read	0	HSOD[6:0]							05h

Page 1 Command Set		82h : Synchronization Timing Adjust 3								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	0	0	0	1	0	82h
1st Parameter	Write / Read	HSOHW[7:0]								19h

Page 1 Command Set		A0h~AFh : PGAMCTRL1~16 (Positive Gamma Control 1~16)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
A0h	Write / Read	0	0	VP0[5:0]						00h
A1h	Write / Read	0	0	VP4[5:0]						0Fh
A2h	Write / Read	0	0	VP8[5:0]						19h
A3h	Write / Read	0	0	0	VP16[4:0]					12h
A4h	Write / Read	0	0	0	VP24[4:0]					13h
A5h	Write / Read	0	0	0	VP52[4:0]					1Ah
A6h	Write / Read	0	0	0	0	VP80[3:0]				0Dh
A7h	Write / Read	0	0	0	0	VP108[3:0]				0Ch
A8h	Write / Read	0	0	0	0	VP147[3:0]				00h
A9h	Write / Read	0	0	0	0	VP175[3:0]				04h
AAh	Write / Read	0	0	0	VP203[4:0]					04h
ABh	Write / Read	0	0	0	VP231[4:0]					0Dh
ACh	Write / Read	0	0	0	VP239[4:0]					0Bh
ADh	Write / Read	0	0	VP247[5:0]						2Ah
AEh	Write / Read	0	0	VP251[5:0]						20h
AFh	Write / Read	0	0	VP255 [5:0]						00h

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Page 1 Command Set		C0h~CFh : NGAMCTRL1~16(Negative Gamma Correction 1~16)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
C0h	Write / Read	0	0	VN0[5:0]						00h
C1h	Write / Read	0	0	VN4[5:0]						0Fh
C2h	Write / Read	0	0	VN8[5:0]						19h
C3h	Write / Read	0	0	0	VN16[4:0]					12h
C4h	Write / Read	0	0	0	VN24[4:0]					13h
C5h	Write / Read	0	0	0	VN52[4:0]					1Ah
C6h	Write / Read	0	0	0	0	VN80[3:0]				0Dh
C7h	Write / Read	0	0	0	0	VN108[3:0]				0Ch
C8h	Write / Read	0	0	0	0	VN147[3:0]				00h
C9h	Write / Read	0	0	0	0	VN175[3:0]				04h
CAh	Write / Read	0	0	0	VN203[4:0]					04h
CBh	Write / Read	0	0	0	VN231[4:0]					0Dh
CCh	Write / Read	0	0	0	VN239[4:0]					0Bh
CDh	Write / Read	0	0	VN247[5:0]						2Ah
CEh	Write / Read	0	0	VN251[5:0]						20h
CFh	Write / Read	0	0	VN255 [5:0]						00h

Page 1 Command Set		E0h : NVMWR 1 (NV Memory Write 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	0	0	E0h
1st Parameter	Write	PGM_DATA[7:0]								00h

Page 1 Command Set		E1h : NVMWR 2 (NV Memory Write 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	0	1	E1h
1st Parameter	Write	PGM_ADR[7:0] / NVM_READ_ADR[7:0]								00h

Page 1 Command Set		E3h : NVMPKEY 1(NV Memory Protection Key 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	1	1	E3h
1st Parameter	Write	KEY[23:16]								XXh

Page 1 Command Set		E4h : NVMPKEY 2(NV Memory Protection Key 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	1	0	0	E4h
1st Parameter	Write	KEY[15:8]								XXh

Page 1 Command Set		E5h : NVMPKEY 3(NV Memory Protection Key 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	1	0	1	E5h
1st Parameter	Write	KEY[7:0]								XXh

Page 1 Command Set		E6h : RDNVM1 (NV Memory Status Read 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	1	1	0	E6h
1st Parameter	Read	0	0	ID2_MK[2:0]			ID1_ MK [2:0]			00h

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Page 1 Command Set		E7h : RDNVM2 (NV Memory Status Read 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	1	1	1	E7h
1st Parameter	Read	0	0	0	0	0	ID3_MK[2:0]			00h

Page 1 Command Set		E8h : RDNVM3 (NV Memory Status Read 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	1	0	0	0	E8h
1st Parameter	Read	GMAP_MK	GMAN_MK	VCM2_MARK[2:0]			VCM1_MARK[2:0]			00h

Page 1 Command Set		E9h : RDNVM4 (NV Memory Status Read 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	1	0	0	1	E9h
1st Parameter	Read	OTP_BUSY	0	0	0	0	0	0	0	00h

Page 1 Command Set		EAh : RDNVM5 (NV Memory Status Read 5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	1	0	1	0	EAh
1st Parameter	Read	NVM_READ_DATA[7:0]								00h

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4.2.3. Page 2 Command List

Page 2 Command Set		00h~3Fh : DGAMCTRL (Digital Gamma Control 1)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write	RCA0 [3:0]				BCA0 [3:0]				-
01h	Write	RCA1 [3:0]				BCA1 [3:0]				-
02h	Write	RCA2 [3:0]				BCA2 [3:0]				-
:	:	:				:				-
XXh	Write	RCAXX [3:0]				BCAXX [3:0]				-
XX+1h	Write	RCAXX+1 [3:0]				BCAXX+1 [3:0]				-
XX+2h	Write	RCAXX+2 [3:0]				BCAXX+2 [3:0]				-
:	:	:				:				-
3Dh	Write	RCA61 [3:0]				BCA61 [3:0]				-
3Eh	Write	RCA62 [3:0]				BCA62 [3:0]				-
3Fh	Write	RCA63 [3:0]				BCA63 [3:0]				-

Page 2 Command Set		40h : D3GE (Digital 3 Gamma Enable)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	0	0	40h
1st Parameter	Write / Read	0	0	0	0	0	0	0	EN_3G	00h

4.2.4. Page 3 Command List

Page 3 Command Set		00h~7Fh : DGAMCTRL (Digital Gamma Control 2)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write	RFA0 [3:0]				BFA0 [3:0]				-
01h	Write	RFA1 [3:0]				BFA1 [3:0]				-
02h	Write	RFA2 [3:0]				BFA2 [3:0]				-
:	:	:				:				-
XXh	Write	RFAXX [3:0]				BFAXX [3:0]				-
XX+1h	Write	RFA XX+1 [3:0]				BFA XX+1 [3:0]				-
XX+2h	Write	RFA XX+2 [3:0]				BFA XX+2 [3:0]				-
:	:	:				:				-
7Dh	Write	RFA125 [3:0]				BFA125 [3:0]				-
7Eh	Write	RFA126 [3:0]				BFA126 [3:0]				-
7Fh	Write	RFA127 [3:0]				BFA127 [3:0]				-

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4.2.5. Page 4 Command List

Page 4 Command Set		00h~7Fh : DGAMCTRL (Digital Gamma Control 3)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write	RFA128 [3:0]				BFA128 [3:0]				-
01h	Write	RFA129 [3:0]				BFA129 [3:0]				-
02h	Write	RFA130 [3:0]				BFA130 [3:0]				-
:	:	:				:				-
XXh	Write	RFAXX [3:0]				BFAXX [3:0]				-
XX+1h	Write	RFA XX+1 [3:0]				BFA XX+1 [3:0]				-
XX+2h	Write	RFA XX+2 [3:0]				BFA XX+2 [3:0]				-
:	:	:				:				-
7Dh	Write	RFA253 [3:0]				BFA253 [3:0]				-
7Eh	Write	RFA254 [3:0]				BFA254 [3:0]				-
7Fh	Write	RFA255 [3:0]				BFA255 [3:0]				-

4.2.6. Page 5 Command List

Page 5 Command Set		00h : BLCTRL1 (Backlight Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	Write / Read	PWM_DIV[7:0]								E8h

Page 5 Command Set		01h : BLCTRL2 (Backlight Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	1	01h
1st Parameter	Write / Read	THRES_MOV[3:0]				THRES_STILL[3:0]				BBh

Page 5 Command Set		02h : BLCTRL3 (Backlight Control 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	0	02h
1st Parameter	Write / Read	0	0	0	0	THRES_UI[3:0]				0Bh

Page 5 Command Set		03h : BLCTRL4 (Backlight Control 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	1	03h
1st Parameter	Write / Read	DTH_MOV[3:0]				DTH_STILL[3:0]				A8h

Page 5 Command Set		04h : BLCTRL5 (Backlight Control 5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	0	04h
1st Parameter	Write / Read	0	0	0	0	DTH_UI[3:0]				04h

Page 5 Command Set		05h : BLCTRL6 (Backlight Control 6)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	1	05h
1st Parameter	Write / Read	0	DIM_MOV[2:0]			0	DIM_STILL[2:0]			43h

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Page 5 Command Set		06h : BLCTRL7 (Backlight Control 7)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	1	0	06h
1st Parameter	Write / Read	DIM_MIN[3:0]				0	DIM_UI[2:0]			02h

Page 5 Command Set		07h : BLCTRL8 (Backlight Control 8)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	1	1	07h
1st Parameter	Write / Read	LABC_SRE_THR[3:0]				LABC SRE_ ENABLE	LEDONR	LEDON POL	PWM POL	B0h

Page 5 Command Set		09h : BLCTRL9 (Backlight Control 9)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	0	1	09h
1st Parameter	Write / Read	SRECABC BOOSTEN	1	1	1	SRECABC EN	1	0	0	74h

Page 5 Command Set		0Ch : BLCTRL10 (Backlight Control 10)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	0	0	0Ch
1st Parameter	Write / Read	ALS8BIT[7:0]								A0h

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4.2.7. Page 6 Command List

Page 6 Command Set		00h~1Dh : GIPCTRL1 (GIP Control 1)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write / Read	F_TIME_OPT	STV_A_Rise[9:8]		GIP_0_SET0					-
01h	Write / Read	STV_A_Rise[7:0]								-
02h	Write / Read	GIP_0_SET1								-
03h	Write / Read	GIP_0_SET2								-
04h	Write / Read	GIP_0_SET3								-
05h	Write / Read	GIP_0_SET4								-
06h	Write / Read	CLK_A_Rise[10:8]			GIP_0_SET5					-
07h	Write / Read	CLK_A_Rise[7:0]								-
08h	Write / Read	GIP_0_SET6								-
09h	Write / Read	GIP_0_SET7								-
0Ah	Write / Read	GIP_0_SET8								-
0Bh	Write / Read	GIP_0_SET9								-
0Ch	Write / Read	GIP_0_SET10								-
0Dh	Write / Read	GIP_0_SET11								-
0Eh	Write / Read	GIP_0_SET12								-
0Fh	Write / Read	GIP_0_SET13								-
10h	Write / Read	GIP_0_SET14								-
11h	Write / Read	GIP_0_SET15								-
12h	Write / Read	GIP_0_SET16								-
13h	Write / Read	GIP_0_SET17								-
14h	Write / Read	GIP_0_SET18								-
15h	Write / Read	GIP_0_SET19								-
16h	Write / Read	GIP_0_SET20								-
17h	Write / Read	GIP_0_SET21								-
18h	Write / Read	GIP_0_SET22								-
19h	Write / Read	GIP_0_SET23								-
1Ah	Write / Read	GIP_0_SET24								-
1Bh	Write / Read	GIP_0_SET25								-
1Ch	Write / Read	GIP_0_SET26								-
1Dh	Write / Read	GIP_0_SET27								-

Page 6 Command Set		20h~27h : GIPCTRL2 (GIP Control 2)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
20h	Write / Read	GIP_1_SET0								-
21h	Write / Read	GIP_1_SET1								-
22h	Write / Read	GIP_1_SET2								-
23h	Write / Read	GIP_1_SET3								-
24h	Write / Read	GIP_1_SET4								-
25h	Write / Read	GIP_1_SET5								-
26h	Write / Read	GIP_1_SET6								-
27h	Write / Read	GIP_1_SET7								-

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Page 6 Command Set		30h~40h : GIPCTRL3 (GIP Control 3)								
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
30h	Write / Read	GIP_2_SET0								-
31h	Write / Read	GIP_2_SET1								-
32h	Write / Read	GIP_2_SET2								-
33h	Write / Read	GIP_2_SET3								-
34h	Write / Read	GIP_2_SET4								-
35h	Write / Read	GIP_2_SET5								-
36h	Write / Read	GIP_2_SET6								-
37h	Write / Read	GIP_2_SET7								-
38h	Write / Read	GIP_2_SET8								-
39h	Write / Read	GIP_2_SET9								-
3Ah	Write / Read	GIP_2_SET10								-
3Bh	Write / Read	GIP_2_SET11								-
3Ch	Write / Read	GIP_2_SET12								-
3Dh	Write / Read	GIP_2_SET13								-
3Eh	Write / Read	GIP_2_SET14								-
3Fh	Write / Read	GIP_2_SET15								-
40h	Write / Read	GIP_2_SET16								-

Page 6 Command Set		52h : GVLOCTRL 1(GOUT_VGLO Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	0	52h
1st Parameter	Write / Read	0	0	0	1	GOUT_VGLO_SO [3:0]				11h

Page 6 Command Set		53h : GVLOCTRL 2(GOUT_VGLO Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write / Read	0	0	0	1	GOUT_VGLO_DSP[3:0]				10h

Page 6 Command Set		54h : GVHOCTRL (GOUT_VGHO Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	0	54h
1st Parameter	Write / Read	0	GOUT_VGHO[2:0]			GOUT_VGLO_LVD[3:0]				11h

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4.2.8. Page 7 Command List

Page 7 Command Set		00h : CLPCTRL (Clamp Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	Write / Read	0	1	0	1	0	VDH_CLP_EN	0	1	55h

Page 7 Command Set		02h : PWBCTRL (Power Bias control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	0	02h
1st Parameter	Write / Read	0	DDVDL_CLP_ISC [2:0]			0	DDVDH_CLP_ISC [2:0]			01h

Page 7 Command Set		06h : VCLCTRL (VCL Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	1	0	06h
1st Parameter	Write / Read	0	0	0	VCLOPT	0	0	VCL_CLP[1:0]		01h

Page 7 Command Set		17h : VGLREGEN (VGL_REG EN)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	1	1	1	17h
1st Parameter	Write / Read	0	0	1	VGLREG_EN	0	0	1	0	22h

Page 7 Command Set		18h : VREG12EN (VREG1/2OUT ENABLE)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	1	0	0	0	18h
1st Parameter	Write / Read	0	0	0	VREG EN	1	1	0	1	0Dh

Page 7 Command Set		B3h : LVDOP (LVD Option)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	1	0	0	1	1	B3h
1st Parameter	Write / Read	0	0	LVD_OP [1:0]		0	0	0	0	00h

Page 7 Command Set		E1h : TIMECTRL (TIME CONTROL)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	0	1	E1h
1st Parameter	Write / Read	TIME_SHIFT_ERR[3:0]				1	0	0	1	09h

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4.3. Page 0 Command Description

4.3.1. NOP (00h)

Page 0 Command Set		00h : NOP (No Operation)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	-	No parameter								-
Description	This command is an empty command; it does not have any effect on the ILI9806E-2C. X = void									
Restriction	To enable this command, “Page 0 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

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4.3.2. Software Reset (01h)

Page 0 Command Set		01h : SWRESET (Software Reset)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	1	01h
1st Parameter	-	No parameter								-
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) X = void									
Restriction	1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first. 2. It is necessary to wait 5msec before sending a new command following software reset. The display module loads all display suppliers’ factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. The Software Reset command cannot be sent during Sleep Out sequence.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

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4.3.3. Read Number of the Errors on DSI (05h)

Page 0 Command Set		05h : RDNUMED (Read Number of the Errors on DSI)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	1	05h
1st Parameter	Read	P[7:0]								XXh
Description	The parameter tells the number of errors on DSI. The more details of the bits are described as below. P [6..0] bits tells the number of the error. P [7] is set to '1' if there is overflow with P[6..0] bits. P [7...0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after the second parameter information is sent (= The read function is completed).This function always returns P [7...0] = 00h if the parallel MPU interface is selected. X = void									
Restriction	To read this command, "Page 0 Command Set enable register (FFh) " must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default		
	Status	**Default Value**
	Power On Sequence	8'h00
	S/W Reset	8'h00
	H/W Reset	8'h00

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4.3.4. Read Display Power Mode (0Ah)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">0Ah : RDDPM (Read Display Power Mode)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0Ah</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>BSTON</td><td>0</td><td>0</td><td>SLPOUT</td><td>NORON</td><td>DISON</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D7</td><td rowspan="2">Booster Voltage Status</td><td>0</td><td>Booster Off or has a fault.</td></tr>
<tr><td>1</td><td>Booster On and working OK</td></tr>
<tr><td>D6</td><td>Not Defined</td><td>--</td><td>Set to ‘0’</td></tr>
<tr><td>D5</td><td>Not Defined</td><td>--</td><td>Set to ‘0’</td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">Sleep In/Out</td><td>0</td><td>Sleep In Mode</td></tr>
<tr><td>1</td><td>Sleep Out Mode</td></tr>
<tr><td rowspan="2">D3</td><td rowspan="2">Display Normal Mode On/Off</td><td>0</td><td>Display Normal Mode Off.</td></tr>
<tr><td>1</td><td>Display Normal Mode On</td></tr>
<tr><td rowspan="2">D2</td><td rowspan="2">Display On/Off</td><td>0</td><td>Display is Off.</td></tr>
<tr><td>1</td><td>Display is On</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>--</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>--</td><td>Set to ‘0’</td></tr>
</table>
X = void</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h08</td></tr>
<tr><td>S/W Reset</td><td>8’h08</td></tr>
<tr><td>H/W Reset</td><td>8’h08</td></tr>
</table>
</td></tr>
</table>

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4.3.5. Read Display MADCTL (0Bh)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">0Bh : RDDMADCTL (Read Display MADCTL)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>BGR</td><td>0</td><td>SS</td><td>GS</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below.
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td>D7</td><td>Reserved</td><td>0</td><td>Reserved, so it is set to ‘0’</td></tr>
<tr><td>D6</td><td>Reserved</td><td>0</td><td>Reserved, so it is set to ‘0’</td></tr>
<tr><td>D5</td><td>Reserved</td><td>0</td><td>Reserved, so it is set to ‘0’</td></tr>
<tr><td>D4</td><td>Reserved</td><td>0</td><td>Reserved, so it is set to ‘0’</td></tr>
<tr><td rowspan="2">D3</td><td rowspan="2">RGB/BGR Order</td><td>0</td><td>RGB (When MADCTL D3=’0’)</td></tr>
<tr><td>1</td><td>BGR (When MADCTL D3=’1’).</td></tr>
<tr><td>D2</td><td>Reserved</td><td>0</td><td>Reserved, so it is set to ‘0’</td></tr>
<tr><td rowspan="2">D1</td><td rowspan="2">Source scan sequence</td><td>0</td><td>Source output Left to Right</td></tr>
<tr><td>1</td><td>Source output Right to Left</td></tr>
<tr><td rowspan="2">D0</td><td rowspan="2">Gate scan sequence</td><td>0</td><td>Gate output Top to Bottom</td></tr>
<tr><td>1</td><td>Gate output Bottom to Top</td></tr>
</table>
X = void.</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
</table>

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4.3.6. Read Display Pixel Format (0Ch)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">0Ch : RDDCOLMOD (Read Display COLMOD)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td colspan="3">DPI [2:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table><tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr><tr><td>1</td><td>0</td><td>1</td><td>16-bit / pixel</td></tr><tr><td>1</td><td>1</td><td>0</td><td>18-bit / pixel</td></tr><tr><td>1</td><td>1</td><td>1</td><td>24-bit / pixel</td></tr><tr><td colspan="3">Others</td><td>Reserved</td></tr></table>X = void.</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h70</td></tr><tr><td>S/W Reset</td><td>8’h70</td></tr><tr><td>H/W Reset</td><td>8’h70</td></tr></table></td></tr>
</table>

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4.3.7. Read Display Image Mode (0Dh)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">0Dh : RDDIM (Read Display Image Mode)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>INVON</td><td>ALLPON</td><td>ALLPOFF</td><td colspan="3">GCS[2:0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the Image Mode status of the display as described :
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D5</td><td rowspan="2">Inversion On/Off</td><td>0</td><td>Inversion is Off.</td></tr>
<tr><td>1</td><td>Inversion is On.</td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">All Pixels On</td><td>0</td><td>Normal Display</td></tr>
<tr><td>1</td><td>White Display</td></tr>
<tr><td rowspan="2">D3</td><td rowspan="2">All Pixels Off</td><td>0</td><td>Normal Display</td></tr>
<tr><td>1</td><td>Black Display</td></tr>
</table>
<table>
<tr><th>D[2:0]</th><th>Gamma Cure Selection</th><th>Gamma Set (26h) Parameter</th></tr>
<tr><td>000</td><td>Gamma curve 1</td><td>GC0(G2.2)</td></tr>
<tr><td>Others</td><td>Not defined</td><td>Not defined</td></tr>
</table>
X = void.</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

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4.3.8. Read Display Signal Mode (0Eh)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">0Eh : RDDSM (Read Display Signal Mode)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>TEON</td><td>0</td><td>HSON</td><td>VSON</td><td>PCLKON</td><td>DEON</td><td>0</td><td>EODSI</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D7</td><td rowspan="2">Tearing Effect Line On/Off</td><td>0</td><td>Tearing Effect Line Off.</td></tr>
<tr><td>1</td><td>Tearing Effect Line On.</td></tr>
<tr><td>D6</td><td>Reserved</td><td>0</td><td>Reserved, so it is set to ‘0’</td></tr>
<tr><td rowspan="2">D5</td><td rowspan="2">Horizontal Sync. (RGB I/F) On/Off</td><td>0</td><td>HS line is low</td></tr>
<tr><td>1</td><td>HS line is high</td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">Vertical Sync. (RGB I/F) On/Off</td><td>0</td><td>VS line is low</td></tr>
<tr><td>1</td><td>VS line is high</td></tr>
<tr><td rowspan="2">D3</td><td rowspan="2">Pixel Clock (PCLK, RGB I/F) On/Off</td><td>0</td><td>PCLK line is low</td></tr>
<tr><td>1</td><td>PCLK line is high</td></tr>
<tr><td rowspan="2">D2</td><td rowspan="2">DE (Data Enable, RGB I/F) On/Off</td><td>0</td><td>DE Line is low</td></tr>
<tr><td>1</td><td>DE Line is high</td></tr>
<tr><td>D1</td><td>Reserved</td><td>0</td><td>Reserved, so it is set to ‘0’</td></tr>
<tr><td rowspan="2">D0</td><td rowspan="2">Error on DSI,</td><td>0</td><td>No Error on DSI</td></tr>
<tr><td>1</td><td>Error on DSI</td></tr>
</table>
X = void.</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

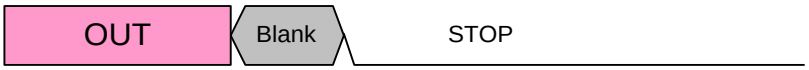
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4.3.9. Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">0Fh : RDDSDR (Read Display Self-Diagnostic Result)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0Fh</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>REGLD</td><td>FUNDT</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the status of the display self-diagnostic results after Sleep Out command as described:
<table>
<tr><th>Bit</th><th>Description</th><th>Action</th></tr>
<tr><td>D7</td><td>Register Loading Detection</td><td>Invert the D7 bit when the OTP and register values are same.</td></tr>
<tr><td>D6</td><td>Functionality Detection</td><td>Invert the D6 bit when the chip met User’s functionality requirements</td></tr>
<tr><td>D5</td><td>Not Used</td><td>Set to ‘0’</td></tr>
<tr><td>D4</td><td>Not Used</td><td>Set to ‘0’</td></tr>
<tr><td>D3</td><td>Not Used</td><td>Set to ‘0’</td></tr>
<tr><td>D2</td><td>Not Used</td><td>Set to ‘0’</td></tr>
<tr><td>D1</td><td>Not Used</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>Not Used</td><td>Set to ‘0’</td></tr>
</table>
X = void.</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

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4.3.10. Sleep In (10h)

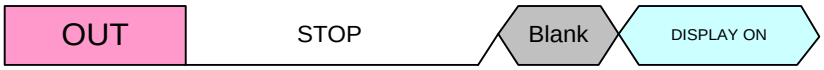
Page 0 Command Set		10h : SLPIN (Sleep In)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	0	10h
1st Parameter	-	No parameter								-
Description	This command causes the ILI9806E-2C to enter the minimum power consumption mode. In this mode the ILI4002 and ILI4003 control signal is stopped, Internal oscillator is stopped, and panel scanning is stopped.  X = Void									
Restriction	1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first. 2. This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to stabilize. It is necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before the Sleep In command can be sent.									
Register Availability										
Default										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

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4.3.11. Sleep Out (11h)

Page 0 Command Set		11h : SLPOUT (Sleep Out)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	0	1	11h
1st Parameter	-	No parameter								-
Description	This command turns off sleep mode. In this mode e.g. the ILI4002 and ILI4003 control signal is enabled, Internal oscillator is started, and panel scanning is started.  X = Void									
Restriction	1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first. 2. This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command (10h), S/W reset command (01h) or H/W reset. It is necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. The ILI9806E-2C loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the ILI9806E-2C is already Sleep Out mode. During this 5msec, ILI9806E-2C is running self-diagnostic functions. It is necessary to wait 120msec after sending the Sleep In command (when in Sleep Out mode) before the Sleep Out command can be sent.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

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4.3.12. Normal Display Mode On (13h)

Page 0 Command Set		13h : NORON (Normal Display Mode On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	0	1	1	13h
1st Parameter	-	No parameter								-
Description	This command returns the display to Normal Display Mode. X = Void									
Restriction	1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first. 2. This command has no effect when Normal Display Mode is active.									
Register Availability										

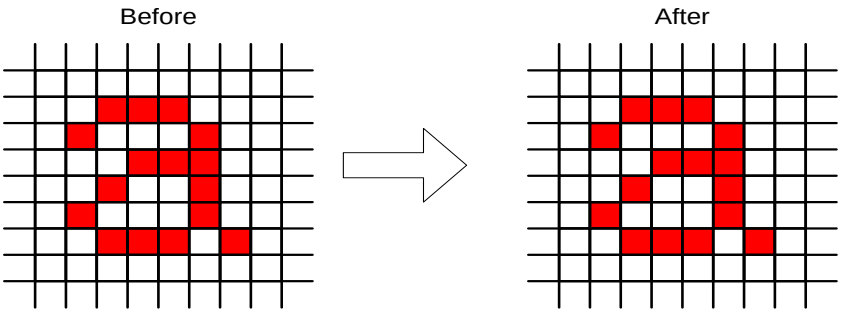
Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
S/W Reset	Normal Display Mode On
H/W Reset	Normal Display Mode On

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4.3.13. Display Inversion Off (20h)

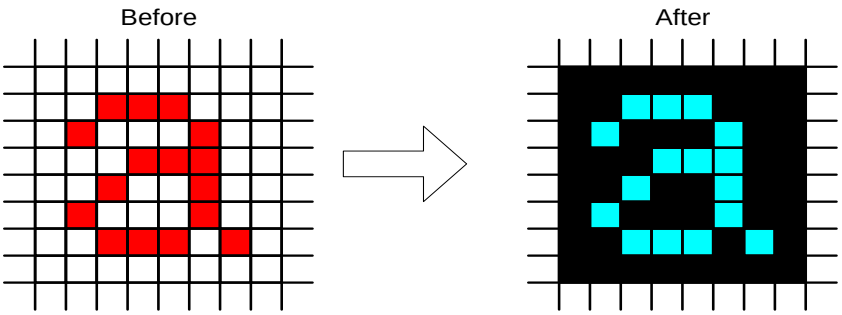
Page 0 Command Set		20h : INVOFF (Display Inversion Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	20h
1st Parameter	-	No parameter								-
Description	This command is used to recover from Display Inversion On mode. This command doesn't change any other status.  X = Void									
Restriction	1. To enable this command, "Page 0 Command Set enable register (FFh) " must set first. 2. This command has no effect when module is already in Display Inversion Off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default		
	Status	**Default Value**
	Power On Sequence	Display Inversion Off
	S/W Reset	Display Inversion Off
	H/W Reset	Display Inversion Off

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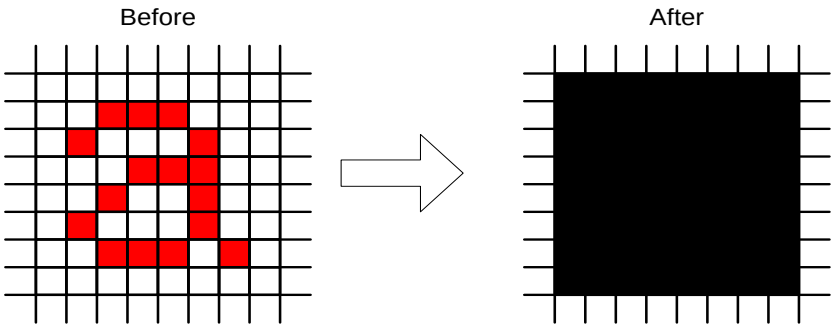
4.3.14. Display Inversion On (21h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">21h : INVON (Display Inversion ON)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21h</td></tr>
<tr><td>1st Parameter</td><td>-</td><td colspan="8">No parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into Display Inversion On mode.
This command doesn't change any other status.
To exit Display Inversion On mode, the Display Inversion Off command (20h) should be written.


X = Void</td></tr>
<tr><td>Restriction</td><td colspan="10">1. To enable this command, "Page 0 Command Set enable register (FFh) " must set first.
2. This command has no effect when the ILI9806E-2C is already in Inversion On mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
</table>

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4.3.15. All Pixel Off (22h)

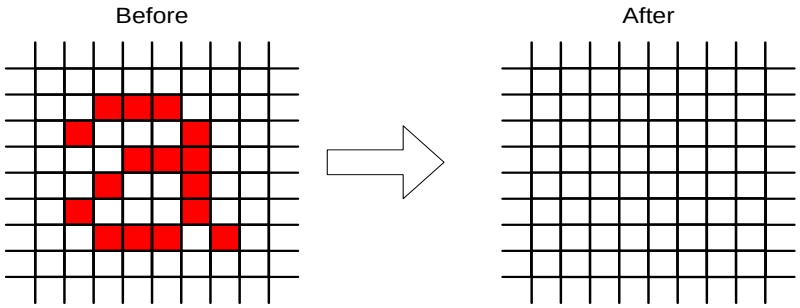
Page 0 Command Set		22h : ALLPOFF (All pixels off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	0	22h
1st Parameter	-	No parameter								-
Description	This command turns the display panel black in 'Sleep Out' mode and a status of the' Display On/Off' register can be 'on' or 'off'. This command does not change any other status  'All Pixels On', 'Normal Display Mode On' commands are used to leave this mode.									
Restriction	1. To enable this command, "Page 0 Command Set enable register (FFh) " must set first. 2. This command has no effect when the ILI9806E-2C is already in All Pixels Off mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default		
	Status	**Default Value**
	Power On Sequence	OFF
	S/W Reset	OFF
	H/W Reset	OFF

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4.3.16. All Pixel On (23h)

Page 0 Command Set		23h : ALLPON (All pixels on)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	1	23h
1st Parameter	-	No parameter								-
Description	This command turns the display panel white in 'Sleep Out ' mode and a status of the 'Display On/Off' register can be 'on' or 'off'. This command does not change any other status.  'All Pixels Off', 'Normal Display Mode On'– commands are used to leave this mode.									
Restriction	1. To enable this command, "Page 0 Command Set enable register (FFh) " must set first. 2. This command has no effect when ILI9806E-2C is already in All Pixels On mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

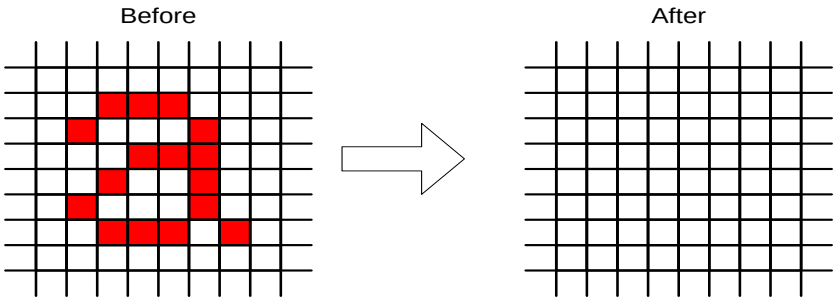
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4.3.17. Gamma Set (26h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">26h : GAMSET (Gamma Set)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>26h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">GC[7:0]</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to select the desired Gamma curve for the current display. A maximum of 1 fixed Gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:
<table>
<tr><th>GC[7:0]</th><th>Parameter</th><th>Curve Selected</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma curve 1 (G2.2)</td></tr>
<tr><td>Others</td><td>Not defined</td><td>Not defined</td></tr>
</table>
Note: All others value are undefined.
X = Void</td></tr>
<tr><td>Restriction</td><td colspan="10">1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first.
2. Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h01</td></tr>
<tr><td>S/W Reset</td><td>8’h01</td></tr>
<tr><td>H/W Reset</td><td>8’h01</td></tr>
</table>
</td></tr>
</table>

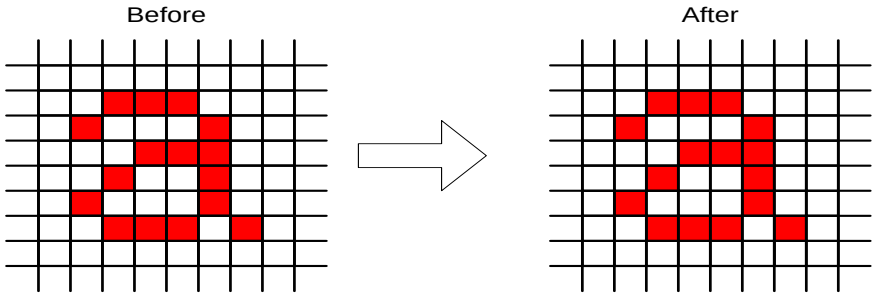
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4.3.18. Display Off (28h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">28h : DISOFF (Display Off)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28h</td></tr>
<tr><td>1st Parameter</td><td>-</td><td colspan="8">No parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page inserted.
This command makes no change any other status.
There will be no abnormal visible effect on the display.

X = Void</td></tr>
<tr><td>Restriction</td><td colspan="10">1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first.
2. This command has no effect when module is already in Display Off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Off</td></tr><tr><td>S/W Reset</td><td>Display Off</td></tr><tr><td>H/W Reset</td><td>Display Off</td></tr></table></td></tr>
</table>

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4.3.19. Display ON (29h)

Page 0 Command Set		29h : DISON (Display ON)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	1	29h
1st Parameter	-	No parameter								-
Description	This command is used to recover from Display Off mode. Output data is enabled. This command does not change any other status.  X = Void									
Restriction	1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first. 2. This command has no effect when the ILI9806E-2C is already in Display on mode.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default		
	Status	**Default Value**
	Power On Sequence	Display Off
	S/W Reset	Display Off
	H/W Reset	Display Off

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4.3.20. Tearing Effect Line Off (34h)

Page 0 Command Set		34h : TEOFF (Tearing Effect Line Off)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	0	34h
1st Parameter	-	No parameter								-
Description	This command is used to turn off the Display module's Tearing Effect output signal (Active Low) from the TE signal line.									
Restriction	1. To enable this command, "Page 0 Command Set enable register (FFh) " must set first. 2. This command has no effect when the Tearing Effect output is already off.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Line Off
S/W Reset	Tearing Effect Line Off
H/W Reset	Tearing Effect Line Off

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4.3.21. Tearing Effect Line On (35h)

Page 0 Command Set		35h : TEON (Tearing Effect Line On)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	1	35h
1st Parameter	-	No parameter								-
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. X = Void									
Restriction	1. To enable this command, “Page 0 Command Set enable register (FFh) ” must set first. 2. This command has no effect when the Tearing Effect output is already ON.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Line Off
S/W Reset	Tearing Effect Line Off
H/W Reset	Tearing Effect Line Off

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4.3.22. Display Access Control (36h)

Page 0 Command Set		36h : Display Access Control								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	1	0	36h
1st Parameter	Write	0	0	0	0	BGR	0	SS	GS	00h

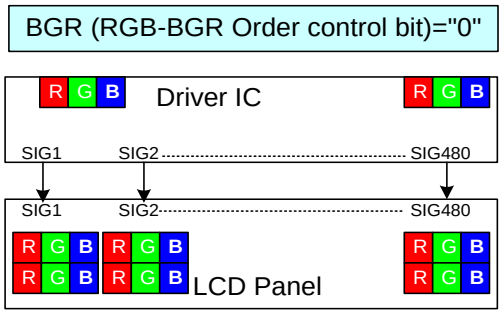
Description

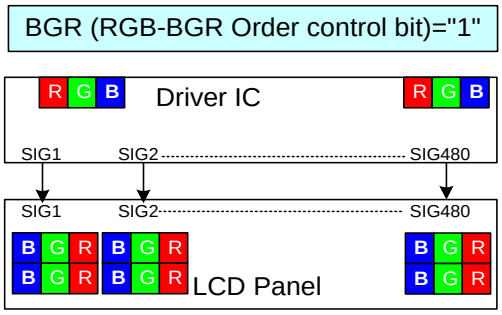
This command defines the panel operation mode

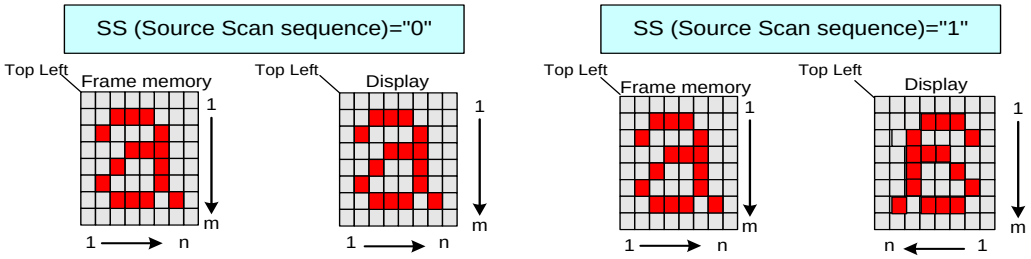
Symbol	Name	Description
BGR	Panel RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
SS	Panel Flip Horizontal	Select the Source driver scan direction on panel module
GS	Panel Flip Vertical	Select the Gate driver scan direction on panel module

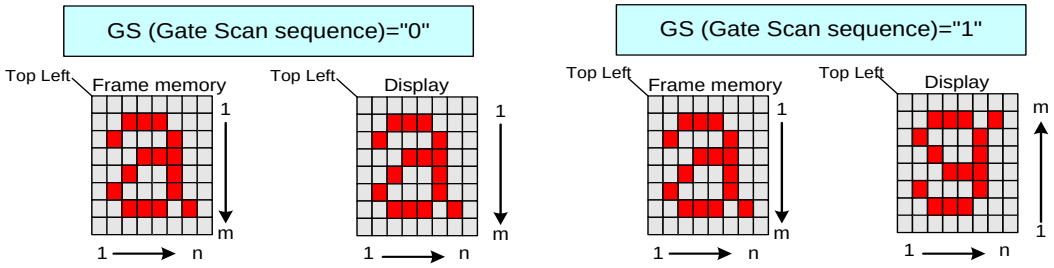
Note : GS scan direction depend on panel's design.

Top-Left (0,0) means the physical panel location









Restriction	To enable this command, "Page 0 Command Set enable register (FFh) " must set first.

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<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>BGR_</th><th>SS</th><th>GS</th></tr>
<tr><td>Power On Sequence</td><td>1b’0</td><td>1b’0</td><td>1b’0</td></tr>
<tr><td>S/W Reset</td><td>1b’0</td><td>1b’0</td><td>1b’0</td></tr>
<tr><td>H/W Reset</td><td>1b’0</td><td>1b’0</td><td>1b’0</td></tr>
</table>
</td></tr>
</table>

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4.3.23. Interface Pixel Format (3Ah)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">3Ah : COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td>0</td><td colspan="3">DPI[2:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70h</td></tr>
<tr><td>Description</td><td colspan="10">This command sets the pixel format. DPI [3:0] selects the pixel format of RGB interface.
<table>
<tr><th colspan="3">DPI[2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18-bit / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24-bit / pixel</td></tr>
</table>
X = void</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h70</td></tr>
<tr><td>S/W Reset</td><td>8’h70</td></tr>
<tr><td>H/W Reset</td><td>8’h70</td></tr>
</table></td></tr>
</table>

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4.3.24. Write Display Brightness Value (51h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">51h : WRDISBV (Write Display Brightness)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">DBV[7:0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to adjust the brightness value of the display.
DBV[7:0]: 8 bit, for display brightness of manual brightness setting and CABC in the ILI9806E-2C. There is a PWM output signal, LEDPWM pin, to control the LED driver IC in order to control display brightness.</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

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4.3.25. Read Display Brightness Value (52h)

Page 0 Command Set		52h : RDDISBV (Read Display Brightness Value)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	0	52h
1st Parameter	Read	DBV[7:0]								XXh
Description	This command is used to return the brightness value of the display. DBV[7:0] is reset when display is in Sleep In mode. DBV[7:0] is '0' when bit BCTRL of "Write CTRL Display (53h)" command is '0'. DBV[7:0] is manual set brightness specified with "Write CTRL Display (53h)" command when BCTRL bit is '1'. When bit BCTRL of "Write CTRL Display (53h)" command is '1' and D1/D0 bit of "Write Content Adaptive Brightness Control (55h)" command are '0', DBV[7:0] output is the brightness value specified with " Write Display Brightness (51h)" command.									
Restriction	To read this command, "Page 0 Command Set enable register (FFh) " must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

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4.3.26. Write CTRL Display Value (53h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">53h : WRCTRLD (Write Control Display)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td>X</td><td>X</td><td>BCTRL</td><td>X</td><td>DD</td><td>BL</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

BCTRL | Description
0 | Brightness Control Block Off (DBV 7:0]=00h)
1 | Brightness Control Block On (DBV[7:0] is active)

DD: Display Dimming Control. This function is only for manual brightness setting.

DD | Description
0 | Display Dimming Off
1 | Display Dimming On

BL: Backlight Control On/Off

BL | Description
0 | Backlight Control Off
1 | Backlight Control On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if Display Dimming On (DD=1) are selected.

X = void</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">Status | Availability
Normal Mode On, Sleep Out | Yes
Sleep Out | Yes
Sleep In | Yes</td></tr>
<tr><td>Default</td><td colspan="10">Status | Default Value
Power On Sequence | 8’h00
S/W Reset | 8’h00
H/W Reset | 8’h00</td></tr>
</table>

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4.3.27. Read CTRL Display Value (54h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">54h : RDCTRLD (Read Control Display Value)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>54h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>X</td><td>X</td><td>BCTRL</td><td>X</td><td>DD</td><td>BL</td><td>X</td><td>X</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.
<table><tr><th>BCTRL</th><th>Description</th></tr><tr><td>0</td><td>Brightness Control Block Off (DBV[7:0]=00h)</td></tr><tr><td>1</td><td>Brightness Control Block On (DBV[7:0] is active)</td></tr></table>DD: Display Dimming Control. This function is only for manual brightness setting.<table><tr><th>DD</th><th>Description</th></tr><tr><td>0</td><td>Display Dimming Off</td></tr><tr><td>1</td><td>Display Dimming On</td></tr></table>BL: Backlight Control On/Off<table><tr><th>BL</th><th>Description</th></tr><tr><td>0</td><td>Backlight Control Off</td></tr><tr><td>1</td><td>Backlight Control On</td></tr></table>X = Void</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

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4.3.28. Write Content Adaptive Brightness Control Value (55h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="8">55h : WRCABC (Write Content Adaptive Brightness Control)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>55h</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="4">C[7:4]</td><td colspan="4">C[3:0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to set parameters for image content based adaptive brightness control functionality.

There are 4 different modes for content adaptive image functionality. These mode are defined in the table below.
<table>
<tr><th colspan="4">C[3:0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>CABC Off</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>User Interface Image mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Still Picture mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Moving Image mode</td></tr>
<tr><td colspan="4">Other Setting</td><td>Prohibited</td></tr>
</table>

Color enhancement level selection.
<table>
<tr><th colspan="4">C [7:4]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Enhancement Disable</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Low Enhancement</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Medium Enhancement</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>High Enhancement</td></tr>
<tr><td colspan="4">Other Setting</td><td>Prohibited</td></tr>
</table>
X = Void</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>C[7:4]</th><th>C[3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’h0</td><td>4’h0</td></tr>
<tr><td>S/W Reset</td><td>4’h0</td><td>4’h0</td></tr>
<tr><td>H/W Reset</td><td>4’h0</td><td>4’h0</td></tr>
</table>
</td></tr>
</table>

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4.3.29. Read Content Adaptive Brightness Control Value (56h)

<table>
<tr><th colspan="2">Page 0 Command Set</th><th colspan="9">56h : RDCABC (Read Content Adaptive Brightness Control)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>56h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="4">C[7:4]</td><td colspan="4">C[3:0]</td><td>XXh</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to read the settings for image content based adaptive brightness control functionality. There are 4 different modes for content adaptive image functionality. These modes are defined in the table below.

<table>
<tr><th colspan="4">C[3:0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>CABC Off</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>User Interface Image mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Still Picture mode</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Moving Image mode</td></tr>
<tr><td colspan="4">Others</td><td>Prohibited</td></tr>
</table>

<table>
<tr><th colspan="4">C [7:4]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Enhancement Disable</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Low Enhancement</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Medium Enhancement</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>High Enhancement</td></tr>
<tr><td colspan="4">Others</td><td>Prohibited</td></tr>
</table>

X = Void</td></tr>
<tr><td>Restriction</td><td colspan="10">To read this command, “Page 0 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>C[7:4]</th><th>C[3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’h0</td><td>4’h0</td></tr>
<tr><td>S/W Reset</td><td>4’h0</td><td>4’h0</td></tr>
<tr><td>H/W Reset</td><td>4’h0</td><td>4’h0</td></tr>
</table>
</td></tr>
</table>

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4.3.30. Write CABC Minimum Brightness (5Eh)

Page 0 Command Set		5Eh : WRCABCMB (Write CABC Minimum Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	1	1	0	5Eh
1st Parameter	Write	CMB[7:0]								XXh
Description	This command is used to set the minimum brightness value of the display for CABC function. **CMB[7:**0]: CABC minimum brightness control, this parameter is used to set a limit to the amount of brightness reduction allowed. When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function works as normal, even if the brightness can not be changed. This function does not affect manual brightness setting. Manual brightness setting does not have a limit on allowable brightness reduction; display brightness can be set less than CABC minimum brightness. Smooth transition and dimming function work as normal. When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. The principle relationship is such that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.									
Restriction	To enable this command, "Page 0 Command Set enable register (FFh) " must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

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4.3.31. Read CABC Minimum Brightness (5Fh)

Page 0 Command Set		5Fh : RDCABCMB (Read CABC Minimum Brightness)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	1	1	1	5Fh
1st Parameter	Read	CMB[7:0]								XXh
Description	This command returns the minimum brightness value of CABC function. The principle relationship is such that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with “Write CABC minimum brightness (5Eh)” command.									
Restriction	To read this command, “Page 0 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	8’h00
S/W Reset	8’h00
H/W Reset	8’h00

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4.3.32. Read automatic brightness control self-diagnostic result (68h)

Page 0 Command Set		68h : RDABCSDR (Read automatic brightness control self-diagnostic result)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	1	0	0	0	68h
1st Parameter	Read	D[7:6]		0	0	0	0	0	0	XXh
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out command as described in the table below: Bit D7 – Register Loading Detection, see section “Register loading Detection ”. Bit D6 – Functionality Detection, see section “Functionality Detection “. Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’.									
Restriction	To read this command, “Page 0 Command Set enable register (FFh) ” must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	2’h0
S/W Reset	2’h0
H/W Reset	2’h0

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4.3.33. Read ID1 (DAh)

Page 0 Command Set		DAh : RDID1 (Read ID1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	0	DAh
1st Parameter	Read	ID1[7:0]								XXh
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is LCD module/driver version ID. The ID1 is programmed by OTP function. X = Void									
Restriction	To read this command, "Page 0 Command Set enable register (FFh) " must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	8'h00	OTP value
H/W Reset	8'h00	OTP value

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4.3.34. Read ID2 (DBh)

Page 0 Command Set		DBh : RDID2 (Read ID2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	0	1	1	DBh
1st Parameter	Read	ID2[7:0]								XXh
Description	This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is LCD module/driver version ID. The ID parameter range is from 80h to FFh. The ID2 is programmed by OTP function. X = Void									
Restriction	To read this command, "Page 0 Command Set enable register (FFh) " must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	8'h80	OTP value
H/W Reset	8'h80	OTP value

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4.3.35. Read ID3 (DCh)

Page 0 Command Set		DCh : RDID3 (Read ID3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	0	1	1	1	0	0	DCh
1st Parameter	Read	ID3[7:0]								XXh
Description	This read byte identifies the LCD module/driver. It is specified by User. The 1st parameter is LCD module/driver ID. The ID3 is programmed by OTP function. X = Void									
Restriction	To read this command, “Page 0 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)	Default Value (After OTP program)
Power On Sequence	8’h00	OTP value
H/W Reset	8’h00	OTP value

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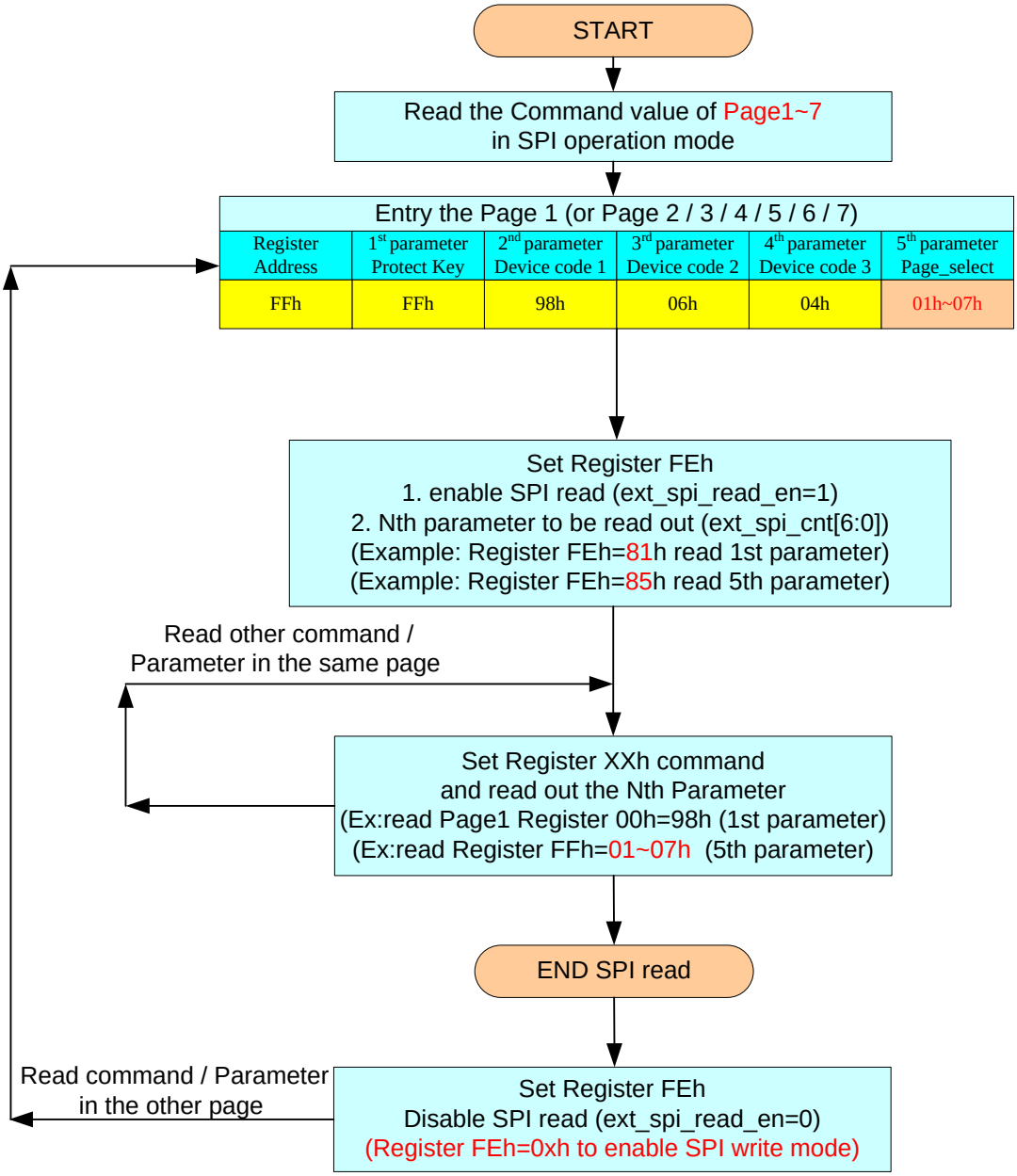
4.3.36. Read EXTC Command In SPI Mode (FEh)

Page 0 Command Set		FEh : RDEXTCSPI(Read EXTC command In SPI)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	1	1	1	1	0	FEh
1st Parameter	Write	ext_spi_read_en	ext_spi_cnt[6:0]							00h

Description

ext_spi_read_en: enable the read function of Page 1/2/3/4/5/6/7 Command and Command FFh in SPI operation mode

ext_spi_cnt[6:0]: the Nth parameter which wants to be read out



Restriction	None

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<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power ON Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
</table>

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4.3.37. EXTC Command Set enable register (FFh)

Page 0 Command Set		FFh : ENEXTC (EXTC command set enable register)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	1	1	1	1	1	FFh
1st Parameter	Write	1	1	1	1	1	1	1	1	FFh
2nd Parameter	Write	1	0	0	1	1	0	0	0	98h
3rd Parameter	Write	0	0	0	0	0	1	1	0	06h
4th Parameter	Write	0	0	0	0	0	1	0	0	04h
5th Parameter	Write / Read	Page [7:0]								00h
Description	Set the register, 1st Parameter=FFh, 2nd Parameter=98h, 3rd Parameter=06h , 4th Parameter=04h , 5th Parameter= Page value to enable “Page command set” available Set the register, 1st Parameter= any value except for FFh, 2nd Parameter= any value except for 98h, 3rd Parameter= any value except for 06h , 4th Parameter= any value except for 04h , 5th Parameter= any value, The “Page command set” is unanailable. See Figure 94. “Command Flow”.									
Restriction	None									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power ON Sequence	40’h0000000000
S/W Reset	40’h0000000000
H/W Reset	40’h0000000000

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4.4. Page 1 Command Description

4.4.1. Read Device Code (00h~02h)

Page 1 Command Set		00h :RDID4 (Read ID 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	Read	ID4 [23 :16]								98h

Page 1 Command Set		01h : RDID4 (Read ID 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	1	01h
1st Parameter	Read	ID4 [15 :8]								06h

Page 1 Command Set		02h : RDID4 (Read ID 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	0	02h
1st Parameter	Read	ID4 [7 :0]								04h
Description	**ID4 [23:0] :** mean the IC model name.									
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	ID4 [23 :0]
Power ON Sequence	24’h980604
S/W Reset	24’h980604
H/W Reset	24’h980604

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4.4.2. Interface Mode Control 1 (08h)

Page 1 Command Set		08h : IFMODE 1(Interface Mode Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	0	0	08h
1st Parameter	Write / Read	0	0	0	SDO_STATUS	SEPT_SDIO	0	0	0	08h
Description	**SEPT_SDIO :** SEPT_SDIO =0: SPI interface transfer data through SDA pin. SEPT_SDIO =1: SPI interface transfer data through SDI and SDO pins. **SDO_STATUS :** SDO_STATUS =0: SDO has output enable , SDO pin output tri-state after data hold time period (timing “toh”). SDO_STATUS =1: always output , but without output tri-state.									
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SDO_STATUS	SEPT_SDIO
Power ON Sequence	1’h0	1’h1
S/W Reset	No Change	No Change
H/W Reset	1’h0	1’h1

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4.4.3. Interface Mode Control 2 (0Ah)

Page 1 Command Set		0Ah : IFMODE 2(Interface Mode Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	1	0	0Ah
1st Parameter	Write / Read	0	0	0	0	0	0	0	2LANE_En	00h

Description

2LANE_EN : Enable Data Lane1

LANSEL	2LANE_En	Description
0	0	Disable Data Lane1
	1	Enable Data Lane1
1	0	Enable Data Lane1
	1	Enable Data Lane1

Restriction

1. To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.
2. In MIPI Interface, when user writes this command, must in the LP mode.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	2LANE_En
Power ON Sequence	1’h0
S/W Reset	No Change
H/W Reset	1’h0

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4.4.4. Display Function Control 1 (20h)

Page 1 Command Set		20h : DISCTRL1 (Display Function Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	0	20h
1st Parameter	Write / Read	0	0	0	0	0	0	0	SYNC MODE	00h
Description	**SYNC_MODE:** Select the operation mode of RGB interface SYNC_MODE: 0 — DE mode; 1 — SYNC mode									
Restriction	To enable this command, "Page 1 Command Set enable register (FFh) " must set first.									
Register Availability	Status: Normal Mode On, Sleep Out — Availability: Yes Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes									
Default	Status: Power ON Sequence — Default Value (SYNC Mode): 1'h0 Status: S/W Reset — Default Value (SYNC Mode): No Change Status: H/W Reset — Default Value (SYNC Mode): 1'h0									

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4.4.5. Display Function Control 2 (21h)

Page 1 Command Set		21h : DISCTRL2 (Display Function Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	0	1	21h
1st Parameter	Write / Read	0	0	0	0	VSPL	HSPL	DPL	EPL	01h
Description	Sets the operation status of the RGB interface. The setting becomes effective as soon as the command is received. **EPL**: DE polarity ("0"= Low enable, "1"= High enable) **DPL**: PCLK polarity set ("0"=data fetched at the rising time, "1"=data fetched at the falling time) **HSPL**: HS polarity ("0"=Low level sync clock, "1"=High level sync clock) **VSPL**: VS polarity ("0"= Low level sync clock, "1"= High level sync clock)									
Restriction	To enable this command, "Page 1 Command Set enable register (FFh) " must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	VSPL	HSPL	DPL	EPL
Power ON Sequence	1'h0	1'h0	1'h0	1'h1
S/W Reset	No Change	No Change	No Change	No Change
H/W Reset	1'h0	1'h0	1'h0	1'h1

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4.4.6. Panel Control 1 (22h)

Page 1 Command Set		22h : PANELCTRL1 (Set panel operation mode1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	0	22h
1st Parameter	Write / Read	0	0	0	0	BGR_ Panel	0	SS_ Panel	GS_ Panel	00h

Description

This command defines the panel operation mode

BGR_Panel:

Symbol	Name	Description
BGR_ Panel	Panel RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)

SS_ Panel: Select the shift direction of outputs from the source driver.

SS_ Panel	Source Output Scan Direction
0	S0 → S1441
1	S1441 → S0

GS_ Panel: Select the shift direction of outputs from the gate driver.

GS_ Panel	Gate Output Scan Direction
0	Top → Bottom
1	Bottom → Top

Note : GS_Panel scan direction depends on panel's design.

Restriction

To enable this command, "Page 1 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BGR_ Panel	SS_ Panel	GS_ Panel
Power On Sequence	1'h0	1'h0	1'h0
S/W Reset	No Change	No Change	No Change
H/W Reset	1'h0	1'h0	1'h0

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4.4.7. Panel Control 2 (23h)

Page 1 Command Set		23h : PANELCTRL2 (Set panel operation mode2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	0	1	1	23h
1st Parameter	Write / Read	0	0	0	0	0	0	REV	0	00h

Description

This command defines the panel operation mode

REV: Normally white or normally black panel select.

NBWSEL	REV	Panel	Data	Color	Source
0	0	normally white	0x00	Black	Largest gamma voltage
			0xFF	White	Smallest gamma voltage
	1	Normally black	0x00	Black	Smallest gamma voltage
			0xFF	White	Largest gamma voltage
1	0	Normally black	0x00	Black	Smallest gamma voltage
			0xFF	White	Largest gamma voltage
	1	Normally black	0x00	Black	Smallest gamma voltage
			0xFF	White	Largest gamma voltage

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	REV
Power On Sequence	1’h0
S/W Reset	No Change
H/W Reset	1’h0

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4.4.8. Data Complement Setting (24h)

Page 1 Command Set		24h : Data Complement Setting								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	0	0	24h
1st Parameter	Write / Read	0	0	0	0	0	0	EPF[1:0]		03h

Description

EPF[1:0]: Set the data format from 16/18-bit (R,G,B) to 24-bit (r, g, b) that is mapping into the internal circuit.

EPF [1:0]	Expand 16-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)	Expand 18-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)
00	"0" is written to the LSB. 8 bits subpixel, data r[7:0]={ 16-bit color data R[4:0], 3'h0 } 8 bits subpixel, data g[7:0]={ 16-bit color data G[5:0], 2'h0 } 8 bits subpixel, data b[7:0]={ 16-bit color data B[4:0], 3'h0 } (Note3): that the data are converted as follows. 16-bit color data R[4:0] =5'h1F, G[5:0]=6'h3F, B[4:0]=5'h1F → 24-bit pixel data r,g,b [7:0]=24'hFFFFFF	"0" is written to the LSB. 8 bits subpixel, data r[7:0]={ 18-bit color data R[5:0], 2'h0 } 8 bits subpixel, data g[7:0]={ 18-bit color data G[5:0], 2'h0 } 8 bits subpixel, data b[7:0]={ 18-bit color data B[5:0], 2'h0 } (Note1): that the data are converted as follows. 18-bit color data R[5:0] =6'h3F, G[5:0]=6'h3F ,B[5:0]=6'h3F → 24-bit pixel data r,g,b [7:0]=24'hFFFFFF
01	"1" is written to the LSB. 8 bits subpixel, data r [7:0]={ 16-bit color data R [4:0], 3'h7 } 8 bits subpixel, data g [7:0]={ 16-bit color data G [5:0], 2'h3 } 8 bits subpixel, data b [7:0]={ 16-bit color data B [4:0], 3'h7 } (Note4): that the data are converted as follows. 16-bit color data R [4:0]=5'h0, G[5:0]=6'h0, B [4:0]=5'h0 →24-bit pixel data r,g,b [7:0]=24'h000000	"1" is written to the LSB. 8 bits subpixel, data r[7:0]={ 18-bit color data R[5:0], 2'h3 } 8 bits subpixel, data g[7:0]={ 18-bit color data G[5:0], 2'h3 } 8 bits subpixel, data b[7:0]={ 18-bit color data B[5:0], 2'h3 } (Note2): that the data are converted as follows. 18-bit color data R [5:0] =6'h0, G [5:0]=6'h0, B [5:0]=6'h0 →24-bit pixel data r,g,b [7:0]=24'h000000
10	The MSB value is written to the LSB. 8 bits subpixel, data r[7:0]={ 16-bit color data R[4:0], R [4:2] } 8 bits subpixel, data g[7:0]={ 16-bit color data G[5:0], G [5:4] } 8 bits subpixel, data b[7:0]={ 16-bit color data B[4:0], B [4:2] }	The MSB value is written to the LSB. 8 bits subpixel, data r[7:0]={ 18-bit color data R[5:0], R [5:4] } 8 bits subpixel, data g[7:0]={ 18-bit color data G[5:0], G [5:4] } 8 bits subpixel, data b[7:0]={ 18-bit color data B[5:0], B [5:4] }
11	Same as setting "EPF [1:0]=10"	Same as setting "EPF [1:0]=10"

Restriction

To enable this command, "Page 1 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	EPF[1:0]
Power ON Sequence	2'h3
S/W Reset	No Change
H/W Reset	2'h3

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4.4.9. Blanking Porch Control1 (25h)

<table>
<tr><th colspan="2">Page 1 Command Set</th><th colspan="9">25h : BLKPRH 1 (Blanking Porch 1)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>25h</td></tr>
<tr><td>1st Parameter</td><td>Write / Read</td><td>0</td><td colspan="7">VFP[6:0]</td><td>14h</td></tr>
<tr><td>Description</td><td colspan="10">VFP[6:0] : The VFP[6:0] bits specify the line number of vertical front porch period respectively.
<table>
<tr><th>VFP[6:0]</th><th>Number of HS of front porch (Dec.)</th></tr>
<tr><td>0000000</td><td>Setting prohibited</td></tr>
<tr><td>0000001</td><td>Setting prohibited</td></tr>
<tr><td>0000010</td><td>2</td></tr>
<tr><td>0000011</td><td>3</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>001110</td><td>14</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>1111101</td><td>125</td></tr>
<tr><td>1111110</td><td>126</td></tr>
<tr><td>1111111</td><td>127</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">1. To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.
2. Vertical porch : Minimum VLW>=1H, VBP>=1H, VFP>=1H</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VFP[6:0]</th></tr>
<tr><td>Power ON Sequence</td><td>7’h14</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>7’h14</td></tr>
</table></td></tr>
</table>

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4.4.10. Blanking Porch Control 2 (26h)

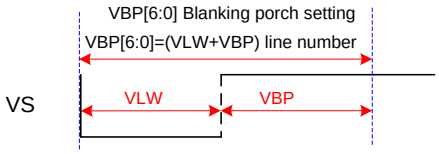
Page 1 Command Set		26h : BLKPRH 2 (Blanking Porch 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	1	0	26h
1st Parameter	Write / Read	0	VBP[6:0]							14h

Description

VBP[6:0] : The VBP[6:0] bits specify the line number of vertical back porch period respectively.

VBP[6:0]	Number of HS of back porch(Dec.)
0000000	Setting prohibited
0000001	Setting prohibited
0000010	2
0000011	3
:	:
001110	14
:	:
1111101	125
1111110	126
1111111	127

We give a illustration of VBP[6:0] setting as below.



Restriction

1. To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.
2. Vertical porch : Minimum VLW>=1H, VBP>=1H, VFP>=1H

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VBP[6:0]
Power ON Sequence	7’h14
S/W Reset	No Change
H/W Reset	7’h14

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4.4.11. Blanking Porch Control 3~4 (27h~28h)

Page 1 Command Set		27h : BLKPRH 3 (Blanking Porch 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	0	1	1	1	27h
1st Parameter	Write / Read	HBP[7:0]								05h

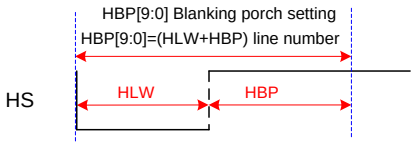
Page 1 Command Set		28h : BLKPRH 4 (Blanking Porch 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	0	1	0	0	0	28h
1st Parameter	Write / Read	0	0	0	0	0	0	HBP[9:8]		00h

Description

HBP[9:0]: The HBP [9:0] bits specify the pclk number of horizontal back porch period respectively.

HBP[9:0]	Number of PCLK of the back porch (Dec.)
0000000000	Setting prohibited
0000000001	Setting prohibited
0000000010	Setting prohibited
0000000011	Setting prohibited
0000000100	Setting prohibited
0000000101	5 (HBP [9:0] default)
:	:
0000010100	20
:	:
0010011110	158
:	:
:	:
1111111101	1021
1111111110	1022
1111111111	1023

We give a illustration of HBP[9:0] setting as below.



Restriction

1. To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.
2. Horizontal porch : Minimum HLW>=1 clock, HBP>=2 clocks , HFP>=2 clocks

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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<table>
<tr>
<td>Default</td>
<td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>HBP[9:0]</th></tr>
<tr><td>Power ON Sequence</td><td>10’h005</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>10’h005</td></tr>
</table>
</td>
</tr>
</table>

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4.4.12. Resolution Control (30h)

<table>
<tr><th colspan="2">Page 1 Command Set</th><th colspan="9">30h : RESCTRL (Resolution Control)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>30h</td></tr>
<tr><td>1st Parameter</td><td>Write / Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">RES[2:0]</td><td>02h</td></tr>
<tr><td>Description</td><td colspan="10">RES[2:0]: These bits are used to select panel resolution.

The relation between bit setting and resolution is illustrated as below table.

<table>
<tr><th>RES[2:0]</th><th>Resolution</th></tr>
<tr><td>000</td><td>480X864</td></tr>
<tr><td>001</td><td>480X854</td></tr>
<tr><td>010</td><td>480X800</td></tr>
<tr><td>011</td><td>480X640</td></tr>
<tr><td>100</td><td>480X720</td></tr>
<tr><td colspan="2">Other setting are inhibited</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>Res[2:0]</th></tr>
<tr><td>Power ON Sequence</td><td>3’h2</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>3’h2</td></tr>
</table></td></tr>
</table>

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4.4.13. Display Inversion Control (31h)

Page 1 Command Set		31h : INVTR (Display Inversion Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	0	0	1	31h
1st Parameter	Write / Read	0	0	0	0	NLA[3:0]				00h

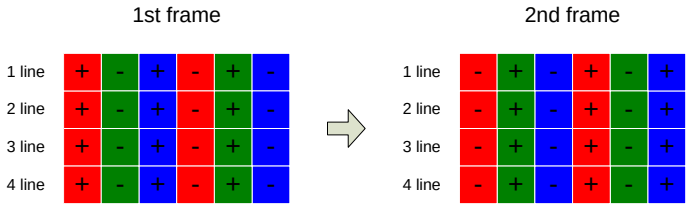
Description

Display inversion mode setting

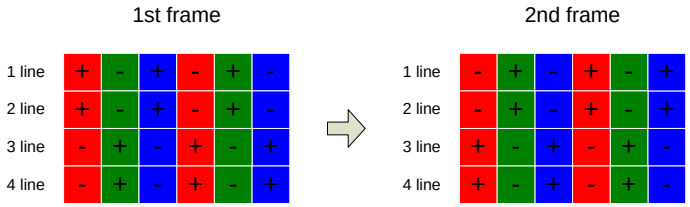
NLA[3:0]: Inversion setting in full colors normal mode (Normal Mode On)

NLA [3:0]				Inversion
0	0	0	0	Column inversion
0	0	1	0	2 dot inversion
Other setting are inhibited				

Column Inversion



2-Dot Inversion



Restriction

To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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<table>
<tr>
<td>Default</td>
<td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>NLA [3:0]</th></tr>
<tr><td>Power ON Sequence</td><td>4’h0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>4’h0</td></tr>
</table>
</td>
</tr>
</table>

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4.4.14. Dithering Enable (34h)

Page 1 Command Set		34h : DITHE (Dithering Enable)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	1	1	0	1	0	0	34h
1st Parameter	Write / Read	0	0	0	0	0	0	0	Dith_en	00h
Description	**Dith_en:** 0 : dithering function disable 1 : dithering function enable									
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	Dith_en
Power ON Sequence	1’h0
S/W Reset	No Change
H/W Reset	1’h0

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4.4.15. Source Signal Adjust (35h)

<table>
<tr><th colspan="2">Page 1 Command Set</th><th colspan="9">35h : Source Signal Adjust</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>1st Parameter</td><td>Write / Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">CHOPPER_SEL_REG[2:0]</td><td>06h</td></tr>
<tr><td>Description</td><td colspan="10">CHOPPER_SEL_REG [2:0]: Source Op-amp chopper function option.

<table>
<tr><th>Chopper_SEL_REG [2]</th><th>Chopper_SEL_REG [1]</th><th>Chopper_SEL_REG [0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>chopper disable</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1 frame chopper</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2 frame chopper</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3 frame chopper</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1 line chopper
(1 frame chopper polarity change)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2 line chopper
(1 frame chopper polarity change)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1 line chopper
(2 frame chopper polarity change)</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2 line chopper
(2 frame chopper polarity change)</td></tr>
</table>

Note: T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>CHOPPER_SEL_REG [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’h6</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>3’h6</td></tr>
</table>
</td></tr>
</table>

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4.4.16. Power Control 1 (40h)

Page 1 Command Set		40h : PWCTRL 1 (Power Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	0	0	40h
1st Parameter	Write / Read	EXB1T	0	EXT_CPCK_SEL[1:0]		BT [3:0]				15h

Description

EXB1T : Selects the external charge pump circuit control for DDVDH and DDVDL.

EXB1T	DDVDH / DDVDL
0	Internal charge pump circuit
1	External charge pump circuit control (ILI4002 and ILI4003)

EXT_CPCK_SEL[1:0] : Pumping clock control signals selection to external control IC (ILI4002 and ILI4003).Set the register before Sleep Out(R11h), when external pumping control is used.

EXT_CPCK_SEL[1:0]		EXTP & EXTN Output
0	0	Output x 1.5 waveform
0	1	Output x 2 waveform
1	0	Output x 3 waveform
1	1	Output Low (power down)

BT[3:0] : DDVDH / DDVDL voltage control

BT[3:0]				DDVDH / DDVDL voltage
0	0	0	0	VCI X 2 / VCI X -2
0	0	0	1	VCI X 2 / VCI X -2.5
0	0	1	0	VCI X 2 / VCI X -3
0	0	1	1	VCI X 2 / VCI X -3
0	1	0	0	VCI X 2.5 / VCI X -2
0	1	0	1	VCI X 2.5 / VCI X -2.5
0	1	1	0	VCI X 2.5 / VCI X -3
0	1	1	1	VCI X 2.5 / VCI X -3
1	0	0	0	VCI X 3 / VCI X -2
1	0	0	1	VCI X 3 / VCI X -2.5
1	0	1	0	VCI X 3 / VCI X -3
1	0	1	1	VCI X 3 / VCI X -3
Other setting are inhibited				

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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Default

Status	Default Value		
	EXB1T	EXT_CPCK_SEL [1:0]	BT [3:0]
Power ON Sequence	1'h0	2'h1	4'h5
S/W Reset	No Change	No Change	No Change
H/W Reset	1'h0	2'h1	4'h5

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4.4.17. Power Control 2 (41h)

Page 1 Command Set		41h : PWCTRL 2 (Power Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	0	1	41h
1st Parameter	Write / Read	0	DDVDH_CLP[2:0]			0	DDVDL_CLP [2:0]			22h

Description

DDVDH_CLP [2:0] : Sets the DDVDH clamp level.

DDVDH_CLP [2:0]			DDVDH clamp level (V)
0	0	0	4.6
0	0	1	4.8
0	1	0	5.0
0	1	1	5.2
1	0	0	5.4
1	0	1	5.6
1	1	0	5.8
1	1	1	6.0

DDVDL_CLP [2:0]: Sets the DDVDL clamp level

DDVDL_CLP [2:0]			DDVDL clamp level (V)
0	0	0	-4.6
0	0	1	-4.8
0	1	0	-5.0
0	1	1	-5.2
1	0	0	-5.4
1	0	1	-5.6
1	1	0	-5.8
1	1	1	-6.0

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

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Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DDVDH_CLP [2:0]	DDVDL_CLP [2:0]
Power ON Sequence	3'h2	3'h2
S/W Reset	No Change	No Change
H/W Reset	3'h2	3'h2

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4.4.18. Power Control 3 (42h)

Page 1 Command Set		42h : PWCTRL 3 (Power Control 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	1	0	42h
1st Parameter	Write / Read	0	0	VGH_CP[1:0]		0	0	VGL_CP[1:0]		02h

Description

VGH_CP [1:0]: Sets the factor used in the step-up circuits for VGH.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

VGH_CP [1:0]		VGH Output
0	0	2DDVDH-DDVDL
0	1	DDVDH+VCIP -DDVDL
1	0	DDVDH+VCIP-VCL
1	1	2DDVDH-DDVDL

VGL_CP [1:0]: Sets the factor used in the step-up circuits for VGL. Select the optimal step-up factor for the operating voltage.

To reduce power consumption, set a smaller factor.

VGL_CP [1:0]		VGL Output
0	0	2DDVDL-DDVDH
0	1	2DDVDL-VCIP
1	0	DDVDL+VCL -VCIP
1	1	DDVDL-DDVDH

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VGH_CP[1:0]	VGL_CP[1:0]
Power ON Sequence	2’h0	2’h2
S/W Reset	No Change	No Change
H/W Reset	2’h0	2’h2

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4.4.19. Power Control 4 (43h)

Page 1 Command Set		43h : PWCTRL 4 (Power Control 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	1	1	43h
1st Parameter	Write / Read	VGH_CLPEN	0	0	0	VGH_CLP[3:0]				09h

Description

VGH _CLPEN: Enable VGH clamp level

VGH _CLPEN	VGH clamp function
0	Disable
1	Enable

VGH_CLP[3:0]: Sets the VGH clamp level

VGH_CLP[3:0]				VGH clamp level (V)
0	0	0	0	10.5
0	0	0	1	11.0
0	0	1	0	11.5
0	0	1	1	12.0
0	1	0	0	12.5
0	1	0	1	13.0
0	1	1	0	13.5
0	1	1	1	14.0
1	0	0	0	14.5
1	0	0	1	15.0
1	0	1	0	15.5
1	0	1	1	16.0
1	1	0	0	16.5
1	1	0	1	17.0
1	1	1	0	17.5
1	1	1	1	18.0

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VGH_CLPEN	VGH_CLP[3:0]
Power ON Sequence	1’h0	4’h9
S/W Reset	No Change	No Change
H/W Reset	1’h0	4’h9

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4.4.20. Power Control 5 (44h)

Page 1 Command Set		44h : PWCTRL 5 (Power Control 5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	0	0	44h
1st Parameter	Write / Read	VGL_CLPEN	0	0	0	VGL_CLP[3:0]				86h

Description

VGL _CLPEN: Enable VGL clamp level

VGL _CLPEN	VGL clamp function
0	Disable
1	Enable

VGL_CLP[3:0]: Sets the VGL clamp level

VGL_CLP[3:0]				VGL clamp level (V)
0	0	0	0	-7.0
0	0	0	1	-7.5
0	0	1	0	-8.0
0	0	1	1	-8.5
0	1	0	0	-9.0
0	1	0	1	-9.5
0	1	1	0	-10.0
0	1	1	1	-11.0
1	0	0	0	-11.5
1	0	0	1	-12.0
1	0	1	0	-12.5
1	0	1	1	-13.0
1	1	0	0	-14.0
1	1	0	1	-14.5
1	1	1	0	-15.0
1	1	1	1	-15.5

Note: The restricted setting VGH – VGL < 32 V.

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VGL_CLPEN	VGL_CLP[3:0]
Power ON Sequence	1’h1	4’h6
S/W Reset	No Change	No Change
H/W Reset	1’h1	4’h6

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4.4.21. Power Control 6 (45h)

Page 1 Command Set		45h : PWCTRL 6 (Power Control 6)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	0	1	45h
1st Parameter	Write / Read	VGH_REG[3:0]				VGL_REG[3:0]				00h

Description

VGH_REG[3:0]: Sets the VGH_REG operating voltage.

VGH_REG[3:0]				. VGH_REG operation voltage (V)
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
0	1	0	0	10.5
0	1	0	1	11.0
0	1	1	0	11.5
0	1	1	1	12.0
1	0	0	0	12.5
1	0	0	1	13.0
1	0	1	0	13.5
1	0	1	1	14.0
1	1	0	0	14.5
1	1	0	1	15.0
1	1	1	0	15.5
1	1	1	1	16.0

VGL_REG[3:0]: Sets the VGL_REG operating voltage.

VGL_REG[3:0]				. VGL_REG operation voltage (V)
0	0	0	0	-7.0
0	0	0	1	-7.5
0	0	1	0	-8.0
0	0	1	1	-8.5
0	1	0	0	-9.0
0	1	0	1	-9.5
0	1	1	0	-10.0
0	1	1	1	-11.0
1	0	0	0	-11.5
1	0	0	1	-12.0
1	0	1	0	-12.5
1	0	1	1	-13.0
1	1	0	0	-14.0
1	1	0	1	-14.5
1	1	1	0	-15.0
1	1	1	1	-15.5

Note : The voltage enable of VGL_REG in Section 4.10.2

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<table>
<tr><td>Restriction</td><td>To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>VGH_REG[3:0]</th><th>VGL_REG[3:0]</th></tr>
<tr><td>Power ON Sequence</td><td>4’h0</td><td>4’h0</td></tr>
<tr><td>S/W Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>4’h0</td><td>4’h0</td></tr>
</table>
</td></tr>
</table>

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4.4.22. Power Control 7 (46h)

<table>
<tr><th colspan="2">Page 1 Command Set</th><th colspan="9">46h : PWCTRL 7 (Power Control 7)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>46h</td></tr>
<tr><td>1st Parameter</td><td>Write / Read</td><td>0</td><td colspan="3">DDVDH_PK1[2:0]</td><td>0</td><td colspan="3">DDVDL_PK 2[2:0]</td><td>33h</td></tr>
<tr><td>Description</td><td colspan="10">
DDVDH_PK1[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking into account the trade-off between the display quality and the current consumption.
<table>
<tr><th colspan="3">DDVDH_PK 1[2:0]</th><th>Step-up cycle for step-up circuit 1</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>16</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Other setting inhibit</td></tr>
</table>
DDVDL_PK 2[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking into account the trade-off between the display quality and the current consumption.
<table>
<tr><th colspan="3">DDVDL_PK 2[2:0]</th><th>Step-up cycle for step-up circuit 2</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>16</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1/2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1/4</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Other setting inhibit</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.</td></tr>
</table>

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Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DDVDH_PK1[2:0]	DDVDL_PK 2[2:0]
Power ON Sequence	3'h3	3'h3
S/W Reset	No Change	No Change
H/W Reset	3'h3	3'h3

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4.4.23. Power Control 8 (47h)

Page 1 Command Set		47h : PWCTRL 8 (Power Control 8)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	1	1	1	47h
1st Parameter	Write / Read	0	VCL_PK3[2:0]			0	VGHL_PK4[2:0]			33h

Description

VCL_PK3[2:0]: Selects the operating frequency of the step-up circuit 3. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking into account the trade-off between the display quality and the current consumption.

VCL_PK 3[2:0]			Step-up cycle for step-up circuit 3
0	0	0	16
0	0	1	8
0	1	0	4
0	1	1	2
1	0	0	1
1	0	1	1/2
1	1	0	1/4
1	1	1	Other setting inhibit

VGHL_PK4[2:0]: Selects the operating frequency of the step-up circuit 4/5. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking into account the trade-off between the display quality and the current consumption.

VGHL_PK 4[2:0]			Step-up cycle for step-up circuit 4/5
0	0	0	16
0	0	1	8
0	1	0	4
0	1	1	2
1	0	0	1
1	0	1	1/2
1	1	0	1/4
1	1	1	Other setting inhibit

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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Default

Status	Default Value	
	VCL_PK3[2:0]	VGHL_PK4[2:0]
Power ON Sequence	3'h3	3'h3
S/W Reset	No Change	No Change
H/W Reset	3'h3	3'h3

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4.4.24. Power Control 9 (50h)

Page 1 Command Set		50h : PWCTRL 9 (Power Control 9)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	0	0	50h
1st Parameter	Write / Read	VREG1[7:0]								78h

Description

VREG1[7:0]: Sets the VREG1OUT voltage for positive Gamma

VREG1[7:0]	VREG1OUT (V)	VREG1[7:0]	VREG1OUT (V)	VREG1[7:0]	VREG1OUT (V)	VREG1[7:0]	VREG1OUT (V)
8'h00	3.0000	8'h40	3.8000	8'h80	4.6000	8'hC0	5.4000
8'h01	3.0125	8'h41	3.8125	8'h81	4.6125	8'hC1	5.4125
8'h02	3.0250	8'h42	3.8250	8'h82	4.6250	8'hC2	5.4250
8'h03	3.0375	8'h43	3.8375	8'h83	4.6375	8'hC3	5.4375
8'h04	3.0500	8'h44	3.8500	8'h84	4.6500	8'hC4	5.4500
8'h05	3.0625	8'h45	3.8625	8'h85	4.6625	8'hC5	5.4625
8'h06	3.0750	8'h46	3.8750	8'h86	4.6750	8'hC6	5.4750
8'h07	3.0875	8'h47	3.8875	8'h87	4.6875	8'hC7	5.4875
8'h08	3.1000	8'h48	3.9000	8'h88	4.7000	8'hC8	5.5000
8'h09	3.1125	8'h49	3.9125	8'h89	4.7125	8'hC9	5.5125
8'h0A	3.1250	8'h4A	3.9250	8'h8A	4.7250	8'hCA	5.5250
8'h0B	3.1375	8'h4B	3.9375	8'h8B	4.7375	8'hCB	5.5375
8'h0C	3.1500	8'h4C	3.9500	8'h8C	4.7500	8'hCC	5.5500
8'h0D	3.1625	8'h4D	3.9625	8'h8D	4.7625	8'hCD	5.5625
8'h0E	3.1750	8'h4E	3.9750	8'h8E	4.7750	8'hCE	5.5750
8'h0F	3.1875	8'h4F	3.9875	8'h8F	4.7875	8'hCF	5.5875
8'h10	3.2000	8'h50	4.0000	8'h90	4.8000	8'hD0	5.6000
8'h11	3.2125	8'h51	4.0125	8'h91	4.8125	8'hD1	5.6125
8'h12	3.2250	8'h52	4.0250	8'h92	4.8250	8'hD2	5.6250
8'h13	3.2375	8'h53	4.0375	8'h93	4.8375	8'hD3	5.6375
8'h14	3.2500	8'h54	4.0500	8'h94	4.8500	8'hD4	5.6500
8'h15	3.2625	8'h55	4.0625	8'h95	4.8625	8'hD5	5.6625
8'h16	3.2750	8'h56	4.0750	8'h96	4.8750	8'hD6	5.6750
8'h17	3.2875	8'h57	4.0875	8'h97	4.8875	8'hD7	5.6875
8'h18	3.3000	8'h58	4.1000	8'h98	4.9000	8'hD8	5.7000
8'h19	3.3125	8'h59	4.1125	8'h99	4.9125	8'hD9	5.7125
8'h1A	3.3250	8'h5A	4.1250	8'h9A	4.9250	8'hDA	5.7250
8'h1B	3.3375	8'h5B	4.1375	8'h9B	4.9375	8'hDB	5.7375
8'h1C	3.3500	8'h5C	4.1500	8'h9C	4.9500	8'hDC	5.7500
8'h1D	3.3625	8'h5D	4.1625	8'h9D	4.9625	8'hDD	5.7625
8'h1E	3.3750	8'h5E	4.1750	8'h9E	4.9750	8'hDE	5.7750
8'h1F	3.3875	8'h5F	4.1875	8'h9F	4.9875	8'hDF	5.7875
8'h20	3.4000	8'h60	4.2000	8'hA0	5.0000	8'hE0	5.8000
8'h21	3.4125	8'h61	4.2125	8'hA1	5.0125	8'hE1	5.8125
8'h22	3.4250	8'h62	4.2250	8'hA2	5.0250	8'hE2	5.8250
8'h23	3.4375	8'h63	4.2375	8'hA3	5.0375	8'hE3	5.8375
8'h24	3.4500	8'h64	4.2500	8'hA4	5.0500	8'hE4	5.8500
8'h25	3.4625	8'h65	4.2625	8'hA5	5.0625	8'hE5	5.8625
8'h26	3.4750	8'h66	4.2750	8'hA6	5.0750	8'hE6	5.8750
8'h27	3.4875	8'h67	4.2875	8'hA7	5.0875	8'hE7	5.8875
8'h28	3.5000	8'h68	4.3000	8'hA8	5.1000	8'hE8	5.9000
8'h29	3.5125	8'h69	4.3125	8'hA9	5.1125	8'hE9	5.9125
8'h2A	3.5250	8'h6A	4.3250	8'hAA	5.1250	8'hEA	5.9250
8'h2B	3.5375	8'h6B	4.3375	8'hAB	5.1375	8'hEB	5.9375
8'h2C	3.5500	8'h6C	4.3500	8'hAC	5.1500	8'hEC	5.9500
8'h2D	3.5625	8'h6D	4.3625	8'hAD	5.1625	8'hED	5.9625
8'h2E	3.5750	8'h6E	4.3750	8'hAE	5.1750	8'hEE	5.9750
8'h2F	3.5875	8'h6F	4.3875	8'hAF	5.1875	8'hEF	5.9875
8'h30	3.6000	8'h70	4.4000	8'hB0	5.2000	8'hF0	6.0000
8'h31	3.6125	8'h71	4.4125	8'hB1	5.2125	8'hF1	6.0125
8'h32	3.6250	8'h72	4.4250	8'hB2	5.2250	8'hF2	6.0250
8'h33	3.6375	8'h73	4.4375	8'hB3	5.2375	8'hF3	6.0375
8'h34	3.6500	8'h74	4.4500	8'hB4	5.2500	8'hF4	6.0500
8'h35	3.6625	8'h75	4.4625	8'hB5	5.2625	8'hF5	6.0625
8'h36	3.6750	8'h76	4.4750	8'hB6	5.2750	8'hF6	6.0750
8'h37	3.6875	8'h77	4.4875	8'hB7	5.2875	8'hF7	6.0875
8'h38	3.7000	8'h78	4.5000	8'hB8	5.3000	8'hF8	6.1000
8'h39	3.7125	8'h79	4.5125	8'hB9	5.3125	8'hF9	6.1125
8'h3A	3.7250	8'h7A	4.5250	8'hBA	5.3250	8'hFA	6.1250
8'h3B	3.7375	8'h7B	4.5375	8'hBB	5.3375	8'hFB	6.1375
8'h3C	3.7500	8'h7C	4.5500	8'hBC	5.3500	8'hFC	6.1500
8'h3D	3.7625	8'h7D	4.5625	8'hBD	5.3625	8'hFD	6.1625
8'h3E	3.7750	8'h7E	4.5750	8'hBE	5.3750	8'hFE	6.1750
8'h3F	3.7875	8'h7F	4.5875	8'hBF	5.3875	8'hFF	6.1875

Note : The voltage enable of VREG1OUT and VREG2OUT is in Sections 4.10.3

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<table>
<tr><td>Restriction</td><td>To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VREG1[7:0]</th></tr>
<tr><td>Power ON Sequence</td><td>8’h78</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>8’h78</td></tr>
</table>
</td></tr>
</table>

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4.4.25. Power Control 10 (51h)

Page 1 Command Set		51h : PWCTRL 10 (Power Control 10)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	0	1	51h
1st Parameter	Write / Read	VREG2[7:0]								78h

Description

VREG2[7:0]: Sets the VREG2OUT voltage for negative Gamma

VREG2[7:0]	VREG2OUT (V)	VREG2[7:0]	VREG2OUT (V)	VREG2[7:0]	VREG2OUT (V)	VREG2[7:0]	VREG2OUT (V)
8'h00	-3.0000	8'h40	-3.8000	8'h80	-4.6000	8'hC0	-5.4000
8'h01	-3.0125	8'h41	-3.8125	8'h81	-4.6125	8'hC1	-5.4125
8'h02	-3.0250	8'h42	-3.8250	8'h82	-4.6250	8'hC2	-5.4250
8'h03	-3.0375	8'h43	-3.8375	8'h83	-4.6375	8'hC3	-5.4375
8'h04	-3.0500	8'h44	-3.8500	8'h84	-4.6500	8'hC4	-5.4500
8'h05	-3.0625	8'h45	-3.8625	8'h85	-4.6625	8'hC5	-5.4625
8'h06	-3.0750	8'h46	-3.8750	8'h86	-4.6750	8'hC6	-5.4750
8'h07	-3.0875	8'h47	-3.8875	8'h87	-4.6875	8'hC7	-5.4875
8'h08	-3.1000	8'h48	-3.9000	8'h88	-4.7000	8'hC8	-5.5000
8'h09	-3.1125	8'h49	-3.9125	8'h89	-4.7125	8'hC9	-5.5125
8'h0A	-3.1250	8'h4A	-3.9250	8'h8A	-4.7250	8'hCA	-5.5250
8'h0B	-3.1375	8'h4B	-3.9375	8'h8B	-4.7375	8'hCB	-5.5375
8'h0C	-3.1500	8'h4C	-3.9500	8'h8C	-4.7500	8'hCC	-5.5500
8'h0D	-3.1625	8'h4D	-3.9625	8'h8D	-4.7625	8'hCD	-5.5625
8'h0E	-3.1750	8'h4E	-3.9750	8'h8E	-4.7750	8'hCE	-5.5750
8'h0F	-3.1875	8'h4F	-3.9875	8'h8F	-4.7875	8'hCF	-5.5875
8'h10	-3.2000	8'h50	-4.0000	8'h90	-4.8000	8'hD0	-5.6000
8'h11	-3.2125	8'h51	-4.0125	8'h91	-4.8125	8'hD1	-5.6125
8'h12	-3.2250	8'h52	-4.0250	8'h92	-4.8250	8'hD2	-5.6250
8'h13	-3.2375	8'h53	-4.0375	8'h93	-4.8375	8'hD3	-5.6375
8'h14	-3.2500	8'h54	-4.0500	8'h94	-4.8500	8'hD4	-5.6500
8'h15	-3.2625	8'h55	-4.0625	8'h95	-4.8625	8'hD5	-5.6625
8'h16	-3.2750	8'h56	-4.0750	8'h96	-4.8750	8'hD6	-5.6750
8'h17	-3.2875	8'h57	-4.0875	8'h97	-4.8875	8'hD7	-5.6875
8'h18	-3.3000	8'h58	-4.1000	8'h98	-4.9000	8'hD8	-5.7000
8'h19	-3.3125	8'h59	-4.1125	8'h99	-4.9125	8'hD9	-5.7125
8'h1A	-3.3250	8'h5A	-4.1250	8'h9A	-4.9250	8'hDA	-5.7250
8'h1B	-3.3375	8'h5B	-4.1375	8'h9B	-4.9375	8'hDB	-5.7375
8'h1C	-3.3500	8'h5C	-4.1500	8'h9C	-4.9500	8'hDC	-5.7500
8'h1D	-3.3625	8'h5D	-4.1625	8'h9D	-4.9625	8'hDD	-5.7625
8'h1E	-3.3750	8'h5E	-4.1750	8'h9E	-4.9750	8'hDE	-5.7750
8'h1F	-3.3875	8'h5F	-4.1875	8'h9F	-4.9875	8'hDF	-5.7875
8'h20	-3.4000	8'h60	-4.2000	8'hA0	-5.0000	8'hE0	-5.8000
8'h21	-3.4125	8'h61	-4.2125	8'hA1	-5.0125	8'hE1	-5.8125
8'h22	-3.4250	8'h62	-4.2250	8'hA2	-5.0250	8'hE2	-5.8250
8'h23	-3.4375	8'h63	-4.2375	8'hA3	-5.0375	8'hE3	-5.8375
8'h24	-3.4500	8'h64	-4.2500	8'hA4	-5.0500	8'hE4	-5.8500
8'h25	-3.4625	8'h65	-4.2625	8'hA5	-5.0625	8'hE5	-5.8625
8'h26	-3.4750	8'h66	-4.2750	8'hA6	-5.0750	8'hE6	-5.8750
8'h27	-3.4875	8'h67	-4.2875	8'hA7	-5.0875	8'hE7	-5.8875
8'h28	-3.5000	8'h68	-4.3000	8'hA8	-5.1000	8'hE8	-5.9000
8'h29	-3.5125	8'h69	-4.3125	8'hA9	-5.1125	8'hE9	-5.9125
8'h2A	-3.5250	8'h6A	-4.3250	8'hAA	-5.1250	8'hEA	-5.9250
8'h2B	-3.5375	8'h6B	-4.3375	8'hAB	-5.1375	8'hEB	-5.9375
8'h2C	-3.5500	8'h6C	-4.3500	8'hAC	-5.1500	8'hEC	-5.9500
8'h2D	-3.5625	8'h6D	-4.3625	8'hAD	-5.1625	8'hED	-5.9625
8'h2E	-3.5750	8'h6E	-4.3750	8'hAE	-5.1750	8'hEE	-5.9750
8'h2F	-3.5875	8'h6F	-4.3875	8'hAF	-5.1875	8'hEF	-5.9875
8'h30	-3.6000	8'h70	-4.4000	8'hB0	-5.2000	8'hF0	-6.0000
8'h31	-3.6125	8'h71	-4.4125	8'hB1	-5.2125	8'hF1	-6.0125
8'h32	-3.6250	8'h72	-4.4250	8'hB2	-5.2250	8'hF2	-6.0250
8'h33	-3.6375	8'h73	-4.4375	8'hB3	-5.2375	8'hF3	-6.0375
8'h34	-3.6500	8'h74	-4.4500	8'hB4	-5.2500	8'hF4	-6.0500
8'h35	-3.6625	8'h75	-4.4625	8'hB5	-5.2625	8'hF5	-6.0625
8'h36	-3.6750	8'h76	-4.4750	8'hB6	-5.2750	8'hF6	-6.0750
8'h37	-3.6875	8'h77	-4.4875	8'hB7	-5.2875	8'hF7	-6.0875
8'h38	-3.7000	8'h78	-4.5000	8'hB8	-5.3000	8'hF8	-6.1000
8'h39	-3.7125	8'h79	-4.5125	8'hB9	-5.3125	8'hF9	-6.1125
8'h3A	-3.7250	8'h7A	-4.5250	8'hBA	-5.3250	8'hFA	-6.1250
8'h3B	-3.7375	8'h7B	-4.5375	8'hBB	-5.3375	8'hFB	-6.1375
8'h3C	-3.7500	8'h7C	-4.5500	8'hBC	-5.3500	8'hFC	-6.1500
8'h3D	-3.7625	8'h7D	-4.5625	8'hBD	-5.3625	8'hFD	-6.1625
8'h3E	-3.7750	8'h7E	-4.5750	8'hBE	-5.3750	8'hFE	-6.1750
8'h3F	-3.7875	8'h7F	-4.5875	8'hBF	-5.3875	8'hFF	-6.1875

Note : The voltage enable of VREG1OUT and VREG2OUT is in Sections 4.10.3

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<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VREG2[7:0]</th></tr>
<tr><td>Power ON Sequence</td><td>8’h78</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>8’h78</td></tr>
</table>
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</table>

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4.4.26. VCOM Control 1~2 (52h~53h)

Page 1 Command Set		52h : VMCTRL1 (VCOM Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	0	52h
1st Parameter	Write / Read	0	0	0	0	0	0	0	VCM1[8]	00h

Page 1 Command Set		53h : VMCTRL2 (VCOM Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write / Read	VCM1[7:0]								6Fh

Description

VCM1 [8:0] is used to set factor to generate VCOM voltage.

VCM1[8:0]	VCOM (V)	VCM1[8:0]	VCOM (V)	VCM1[8:0]	VCOM (V)	VCM1[8:0]	VCOM (V)	VCM1[8:0]	VCOM (V)
9'h000	0.0000	9'h040	-0.9875	9'h080	-1.7875	9'h0C0	-2.5875	9'h100	-3.3875
9'h001	-0.2000	9'h041	-1.0000	9'h081	-1.8000	9'h0C1	-2.6000	9'h101	-3.4000
9'h002	-0.2125	9'h042	-1.0125	9'h082	-1.8125	9'h0C2	-2.6125	9'h102	-3.4125
9'h003	-0.2250	9'h043	-1.0250	9'h083	-1.8250	9'h0C3	-2.6250	9'h103	-3.4250
9'h004	-0.2375	9'h044	-1.0375	9'h084	-1.8375	9'h0C4	-2.6375	9'h104	-3.4375
9'h005	-0.2500	9'h045	-1.0500	9'h085	-1.8500	9'h0C5	-2.6500	9'h105	-3.4500
9'h006	-0.2625	9'h046	-1.0625	9'h086	-1.8625	9'h0C6	-2.6625	9'h106	-3.4625
9'h007	-0.2750	9'h047	-1.0750	9'h087	-1.8750	9'h0C7	-2.6750	9'h107	-3.4750
9'h008	-0.2875	9'h048	-1.0875	9'h088	-1.8875	9'h0C8	-2.6875	9'h108	-3.4875
9'h009	-0.3000	9'h049	-1.1000	9'h089	-1.9000	9'h0C9	-2.7000	9'h109	-3.5000
9'h00A	-0.3125	9'h04A	-1.1125	9'h08A	-1.9125	9'h0CA	-2.7125	9'h10A	-3.5125
9'h00B	-0.3250	9'h04B	-1.1250	9'h08B	-1.9250	9'h0CB	-2.7250	9'h10B	-3.5250
9'h00C	-0.3375	9'h04C	-1.1375	9'h08C	-1.9375	9'h0CC	-2.7375	9'h10C	-3.5375
9'h00D	-0.3500	9'h04D	-1.1500	9'h08D	-1.9500	9'h0CD	-2.7500	9'h10D	-3.5500
9'h00E	-0.3625	9'h04E	-1.1625	9'h08E	-1.9625	9'h0CE	-2.7625	9'h10E	-3.5625
9'h00F	-0.3750	9'h04F	-1.1750	9'h08F	-1.9750	9'h0CF	-2.7750	9'h10F	-3.5750
9'h010	-0.3875	9'h050	-1.1875	9'h090	-1.9875	9'h0D0	-2.7875	9'h110	-3.5875
9'h011	-0.4000	9'h051	-1.2000	9'h091	-2.0000	9'h0D1	-2.8000	9'h111	-3.6000
9'h012	-0.4125	9'h052	-1.2125	9'h092	-2.0125	9'h0D2	-2.8125	9'h112	-3.6125
9'h013	-0.4250	9'h053	-1.2250	9'h093	-2.0250	9'h0D3	-2.8250	9'h113	-3.6250
9'h014	-0.4375	9'h054	-1.2375	9'h094	-2.0375	9'h0D4	-2.8375	9'h114	-3.6375
9'h015	-0.4500	9'h055	-1.2500	9'h095	-2.0500	9'h0D5	-2.8500	9'h115	-3.6500
9'h016	-0.4625	9'h056	-1.2625	9'h096	-2.0625	9'h0D6	-2.8625	9'h116	-3.6625
9'h017	-0.4750	9'h057	-1.2750	9'h097	-2.0750	9'h0D7	-2.8750	9'h117	-3.6750
9'h018	-0.4875	9'h058	-1.2875	9'h098	-2.0875	9'h0D8	-2.8875	9'h118	-3.6875
9'h019	-0.5000	9'h059	-1.3000	9'h099	-2.1000	9'h0D9	-2.9000	9'h119	-3.7000
9'h01A	-0.5125	9'h05A	-1.3125	9'h09A	-2.1125	9'h0DA	-2.9125	9'h11A	-3.7125
9'h01B	-0.5250	9'h05B	-1.3250	9'h09B	-2.1250	9'h0DB	-2.9250	9'h11B	-3.7250
9'h01C	-0.5375	9'h05C	-1.3375	9'h09C	-2.1375	9'h0DC	-2.9375	9'h11C	-3.7375
9'h01D	-0.5500	9'h05D	-1.3500	9'h09D	-2.1500	9'h0DD	-2.9500	9'h11D	-3.7500
9'h01E	-0.5625	9'h05E	-1.3625	9'h09E	-2.1625	9'h0DE	-2.9625	9'h11E	-3.7625
9'h01F	-0.5750	9'h05F	-1.3750	9'h09F	-2.1750	9'h0DF	-2.9750	9'h11F	-3.7750
9'h020	-0.5875	9'h060	-1.3875	9'h0A0	-2.1875	9'h0E0	-2.9875	9'h120	-3.7875
9'h021	-0.6000	9'h061	-1.4000	9'h0A1	-2.2000	9'h0E1	-3.0000	9'h121	-3.8000
9'h022	-0.6125	9'h062	-1.4125	9'h0A2	-2.2125	9'h0E2	-3.0125	9'h122	-3.8125
9'h023	-0.6250	9'h063	-1.4250	9'h0A3	-2.2250	9'h0E3	-3.0250	9'h123	-3.8250
9'h024	-0.6375	9'h064	-1.4375	9'h0A4	-2.2375	9'h0E4	-3.0375	9'h124	-3.8375
9'h025	-0.6500	9'h065	-1.4500	9'h0A5	-2.2500	9'h0E5	-3.0500	9'h125	-3.8500
9'h026	-0.6625	9'h066	-1.4625	9'h0A6	-2.2625	9'h0E6	-3.0625	9'h126	-3.8625
9'h027	-0.6750	9'h067	-1.4750	9'h0A7	-2.2750	9'h0E7	-3.0750	9'h127	-3.8750
9'h028	-0.6875	9'h068	-1.4875	9'h0A8	-2.2875	9'h0E8	-3.0875	9'h128	-3.8875
9'h029	-0.7000	9'h069	-1.5000	9'h0A9	-2.3000	9'h0E9	-3.1000	9'h129	-3.9000
9'h02A	-0.7125	9'h06A	-1.5125	9'h0AA	-2.3125	9'h0EA	-3.1125	9'h12A	-3.9125
9'h02B	-0.7250	9'h06B	-1.5250	9'h0AB	-2.3250	9'h0EB	-3.1250	9'h12B	-3.9250
9'h02C	-0.7375	9'h06C	-1.5375	9'h0AC	-2.3375	9'h0EC	-3.1375	9'h12C	-3.9375
9'h02D	-0.7500	9'h06D	-1.5500	9'h0AD	-2.3500	9'h0ED	-3.1500	9'h12D	-3.9500
9'h02E	-0.7625	9'h06E	-1.5625	9'h0AE	-2.3625	9'h0EE	-3.1625	9'h12E	-3.9625
9'h02F	-0.7750	9'h06F	-1.5750	9'h0AF	-2.3750	9'h0EF	-3.1750	9'h12F	-3.9750
9'h030	-0.7875	9'h070	-1.5875	9'h0B0	-2.3875	9'h0F0	-3.1875	9'h130	-3.9875
9'h031	-0.8000	9'h071	-1.6000	9'h0B1	-2.4000	9'h0F1	-3.2000	9'h131	-4.0000
9'h032	-0.8125	9'h072	-1.6125	9'h0B2	-2.4125	9'h0F2	-3.2125	9'h132	Setting inhibit
9'h033	-0.8250	9'h073	-1.6250	9'h0B3	-2.4250	9'h0F3	-3.2250	9'h133	Setting inhibit
9'h034	-0.8375	9'h074	-1.6375	9'h0B4	-2.4375	9'h0F4	-3.2375	9'h134	Setting inhibit
9'h035	-0.8500	9'h075	-1.6500	9'h0B5	-2.4500	9'h0F5	-3.2500	9'h135	Setting inhibit
9'h036	-0.8625	9'h076	-1.6625	9'h0B6	-2.4625	9'h0F6	-3.2625	9'h136	Setting inhibit
9'h037	-0.8750	9'h077	-1.6750	9'h0B7	-2.4750	9'h0F7	-3.2750	9'h137	Setting inhibit
9'h038	-0.8875	9'h078	-1.6875	9'h0B8	-2.4875	9'h0F8	-3.2875	9'h138	Setting inhibit
9'h039	-0.9000	9'h079	-1.7000	9'h0B9	-2.5000	9'h0F9	-3.3000	9'h139	Setting inhibit
9'h03A	-0.9125	9'h07A	-1.7125	9'h0BA	-2.5125	9'h0FA	-3.3125	9'h13A	Setting inhibit
9'h03B	-0.9250	9'h07B	-1.7250	9'h0BB	-2.5250	9'h0FB	-3.3250	9'h13B	Setting inhibit
9'h03C	-0.9375	9'h07C	-1.7375	9'h0BC	-2.5375	9'h0FC	-3.3375	9'h13C	Setting inhibit

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9'h03D	-0.9500	9'h07D	-1.7500	9'h0BD	-2.5500	9'h0FD	-3.3500	9'h13D	Setting inhibit
9'h03E	-0.9625	9'h07E	-1.7625	9'h0BE	-2.5625	9'h0FE	-3.3625	9'h13E	Setting inhibit
9'h03F	-0.9750	9'h07F	-1.7750	9'h0BF	-2.5750	9'h0FF	-3.3750	9'h13F	Setting inhibit

Note 1: VCOM ≧ VCL + 0.3V

Note 2: GS = 1'b0 , VCOM voltage = VCM1[8:0] setting, GS = 1'b1 VCOM voltage = VCM2[8:0]

Restriction

To enable this command, "Page 1 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VCM1[8]	VCM1[7:0]
Power ON Sequence	1'h0	8'h6F
S/W Reset	No Change	No Change
H/W Reset	1'h0	8'h6F

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4.4.27. VCOM Control 3~4 (54h~55h)

Page 1 Command Set		54h : VMCTRL3 (VCOM Control 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	0	54h
1st Parameter	Write / Read	0	0	0	0	0	0	0	VCM2[8]	00h

Page 1 Command Set		55h : VMCTRL4 (VCOM Control 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	1	55h
1st Parameter	Write / Read	VCM2[7:0]								6Fh

Description

VCM2 [8:0] is used to set factor to generate VCOM voltage.

VCM2[8:0]	VCOM (V)	VCM2[8:0]	VCOM (V)	VCM2[8:0]	VCOM (V)	VCM2[8:0]	VCOM (V)	VCM2[8:0]	VCOM (V)
9'h000	0.0000	9'h040	-0.9875	9'h080	-1.7875	9'h0C0	-2.5875	9'h100	-3.3875
9'h001	-0.2000	9'h041	-1.0000	9'h081	-1.8000	9'h0C1	-2.6000	9'h101	-3.4000
9'h002	-0.2125	9'h042	-1.0125	9'h082	-1.8125	9'h0C2	-2.6125	9'h102	-3.4125
9'h003	-0.2250	9'h043	-1.0250	9'h083	-1.8250	9'h0C3	-2.6250	9'h103	-3.4250
9'h004	-0.2375	9'h044	-1.0375	9'h084	-1.8375	9'h0C4	-2.6375	9'h104	-3.4375
9'h005	-0.2500	9'h045	-1.0500	9'h085	-1.8500	9'h0C5	-2.6500	9'h105	-3.4500
9'h006	-0.2625	9'h046	-1.0625	9'h086	-1.8625	9'h0C6	-2.6625	9'h106	-3.4625
9'h007	-0.2750	9'h047	-1.0750	9'h087	-1.8750	9'h0C7	-2.6750	9'h107	-3.4750
9'h008	-0.2875	9'h048	-1.0875	9'h088	-1.8875	9'h0C8	-2.6875	9'h108	-3.4875
9'h009	-0.3000	9'h049	-1.1000	9'h089	-1.9000	9'h0C9	-2.7000	9'h109	-3.5000
9'h00A	-0.3125	9'h04A	-1.1125	9'h08A	-1.9125	9'h0CA	-2.7125	9'h10A	-3.5125
9'h00B	-0.3250	9'h04B	-1.1250	9'h08B	-1.9250	9'h0CB	-2.7250	9'h10B	-3.5250
9'h00C	-0.3375	9'h04C	-1.1375	9'h08C	-1.9375	9'h0CC	-2.7375	9'h10C	-3.5375
9'h00D	-0.3500	9'h04D	-1.1500	9'h08D	-1.9500	9'h0CD	-2.7500	9'h10D	-3.5500
9'h00E	-0.3625	9'h04E	-1.1625	9'h08E	-1.9625	9'h0CE	-2.7625	9'h10E	-3.5625
9'h00F	-0.3750	9'h04F	-1.1750	9'h08F	-1.9750	9'h0CF	-2.7750	9'h10F	-3.5750
9'h010	-0.3875	9'h050	-1.1875	9'h090	-1.9875	9'h0D0	-2.7875	9'h110	-3.5875
9'h011	-0.4000	9'h051	-1.2000	9'h091	-2.0000	9'h0D1	-2.8000	9'h111	-3.6000
9'h012	-0.4125	9'h052	-1.2125	9'h092	-2.0125	9'h0D2	-2.8125	9'h112	-3.6125
9'h013	-0.4250	9'h053	-1.2250	9'h093	-2.0250	9'h0D3	-2.8250	9'h113	-3.6250
9'h014	-0.4375	9'h054	-1.2375	9'h094	-2.0375	9'h0D4	-2.8375	9'h114	-3.6375
9'h015	-0.4500	9'h055	-1.2500	9'h095	-2.0500	9'h0D5	-2.8500	9'h115	-3.6500
9'h016	-0.4625	9'h056	-1.2625	9'h096	-2.0625	9'h0D6	-2.8625	9'h116	-3.6625
9'h017	-0.4750	9'h057	-1.2750	9'h097	-2.0750	9'h0D7	-2.8750	9'h117	-3.6750
9'h018	-0.4875	9'h058	-1.2875	9'h098	-2.0875	9'h0D8	-2.8875	9'h118	-3.6875
9'h019	-0.5000	9'h059	-1.3000	9'h099	-2.1000	9'h0D9	-2.9000	9'h119	-3.7000
9'h01A	-0.5125	9'h05A	-1.3125	9'h09A	-2.1125	9'h0DA	-2.9125	9'h11A	-3.7125
9'h01B	-0.5250	9'h05B	-1.3250	9'h09B	-2.1250	9'h0DB	-2.9250	9'h11B	-3.7250
9'h01C	-0.5375	9'h05C	-1.3375	9'h09C	-2.1375	9'h0DC	-2.9375	9'h11C	-3.7375
9'h01D	-0.5500	9'h05D	-1.3500	9'h09D	-2.1500	9'h0DD	-2.9500	9'h11D	-3.7500
9'h01E	-0.5625	9'h05E	-1.3625	9'h09E	-2.1625	9'h0DE	-2.9625	9'h11E	-3.7625
9'h01F	-0.5750	9'h05F	-1.3750	9'h09F	-2.1750	9'h0DF	-2.9750	9'h11F	-3.7750
9'h020	-0.5875	9'h060	-1.3875	9'h0A0	-2.1875	9'h0E0	-2.9875	9'h120	-3.7875
9'h021	-0.6000	9'h061	-1.4000	9'h0A1	-2.2000	9'h0E1	-3.0000	9'h121	-3.8000
9'h022	-0.6125	9'h062	-1.4125	9'h0A2	-2.2125	9'h0E2	-3.0125	9'h122	-3.8125
9'h023	-0.6250	9'h063	-1.4250	9'h0A3	-2.2250	9'h0E3	-3.0250	9'h123	-3.8250
9'h024	-0.6375	9'h064	-1.4375	9'h0A4	-2.2375	9'h0E4	-3.0375	9'h124	-3.8375
9'h025	-0.6500	9'h065	-1.4500	9'h0A5	-2.2500	9'h0E5	-3.0500	9'h125	-3.8500
9'h026	-0.6625	9'h066	-1.4625	9'h0A6	-2.2625	9'h0E6	-3.0625	9'h126	-3.8625
9'h027	-0.6750	9'h067	-1.4750	9'h0A7	-2.2750	9'h0E7	-3.0750	9'h127	-3.8750
9'h028	-0.6875	9'h068	-1.4875	9'h0A8	-2.2875	9'h0E8	-3.0875	9'h128	-3.8875
9'h029	-0.7000	9'h069	-1.5000	9'h0A9	-2.3000	9'h0E9	-3.1000	9'h129	-3.9000
9'h02A	-0.7125	9'h06A	-1.5125	9'h0AA	-2.3125	9'h0EA	-3.1125	9'h12A	-3.9125
9'h02B	-0.7250	9'h06B	-1.5250	9'h0AB	-2.3250	9'h0EB	-3.1250	9'h12B	-3.9250
9'h02C	-0.7375	9'h06C	-1.5375	9'h0AC	-2.3375	9'h0EC	-3.1375	9'h12C	-3.9375
9'h02D	-0.7500	9'h06D	-1.5500	9'h0AD	-2.3500	9'h0ED	-3.1500	9'h12D	-3.9500
9'h02E	-0.7625	9'h06E	-1.5625	9'h0AE	-2.3625	9'h0EE	-3.1625	9'h12E	-3.9625
9'h02F	-0.7750	9'h06F	-1.5750	9'h0AF	-2.3750	9'h0EF	-3.1750	9'h12F	-3.9750
9'h030	-0.7875	9'h070	-1.5875	9'h0B0	-2.3875	9'h0F0	-3.1875	9'h130	-3.9875
9'h031	-0.8000	9'h071	-1.6000	9'h0B1	-2.4000	9'h0F1	-3.2000	9'h131	-4.0000
9'h032	-0.8125	9'h072	-1.6125	9'h0B2	-2.4125	9'h0F2	-3.2125	9'h132	Setting inhibit
9'h033	-0.8250	9'h073	-1.6250	9'h0B3	-2.4250	9'h0F3	-3.2250	9'h133	Setting inhibit
9'h034	-0.8375	9'h074	-1.6375	9'h0B4	-2.4375	9'h0F4	-3.2375	9'h134	Setting inhibit
9'h035	-0.8500	9'h075	-1.6500	9'h0B5	-2.4500	9'h0F5	-3.2500	9'h135	Setting inhibit
9'h036	-0.8625	9'h076	-1.6625	9'h0B6	-2.4625	9'h0F6	-3.2625	9'h136	Setting inhibit
9'h037	-0.8750	9'h077	-1.6750	9'h0B7	-2.4750	9'h0F7	-3.2750	9'h137	Setting inhibit
9'h038	-0.8875	9'h078	-1.6875	9'h0B8	-2.4875	9'h0F8	-3.2875	9'h138	Setting inhibit
9'h039	-0.9000	9'h079	-1.7000	9'h0B9	-2.5000	9'h0F9	-3.3000	9'h139	Setting inhibit
9'h03A	-0.9125	9'h07A	-1.7125	9'h0BA	-2.5125	9'h0FA	-3.3125	9'h13A	Setting inhibit
9'h03B	-0.9250	9'h07B	-1.7250	9'h0BB	-2.5250	9'h0FB	-3.3250	9'h13B	Setting inhibit
9'h03C	-0.9375	9'h07C	-1.7375	9'h0BC	-2.5375	9'h0FC	-3.3375	9'h13C	Setting inhibit

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9'h03D	-0.9500	9'h07D	-1.7500	9'h0BD	-2.5500	9'h0FD	-3.3500	9'h13D	Setting inhibit
9'h03E	-0.9625	9'h07E	-1.7625	9'h0BE	-2.5625	9'h0FE	-3.3625	9'h13E	Setting inhibit
9'h03F	-0.9750	9'h07F	-1.7750	9'h0BF	-2.5750	9'h0FF	-3.3750	9'h13F	Setting inhibit

Note 1: VCOM ≧ VCL + 0.3V

Note 2: GS = 1'b0 , VCOM voltage = VCM1[8:0] setting, GS = 1'b1 VCOM voltage = VCM2[8:0]

Restriction

To enable this command, "Page 1 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VCM2[8]	VCM2[7:0]
Power ON Sequence	1'h0	8'h6F
S/W Reset	No Change	No Change
H/W Reset	1'h0	8'h6F

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4.4.28. VCOM Control 5 (56h)

Page 1 Command Set		56h : VMCTRL5 (VCOM Control 5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	1	0	56h
1st Parameter	Write / Read	0	0	0	NVM2	0	0	0	NVM1	00h

Description

NVM1 : Selection of the VCM1 setting.

Program NV Memory for VCM1[8:0]	NVM1	Description
Before	**1'b0**	Register 52h and 53h for VCM1 setting
	1'b1	Setting inhibit
After	**1'b0**	NV Memory selected for VCM1 setting
	1'b1	Register 52h and 53h for VCM1 setting

NVM2 : Selection of the VCM2 setting.

Program NV Memory for VCM2[8:0]	NVM2	Description
Before	**1'b0**	Register 54h and 55h for VCM2 setting
	1'b1	Setting inhibit
After	**1'b0**	NV Memory selected for VCM2 setting
	1'b1	Register 54h and 55h for VCM2 setting

Restriction

1. To enable this command, "Page 1 Command Set enable register (FFh) " must set first.
2. Before the NV memory is programmed, it is prohibited from setting NVM1 / NVM2=1'b1.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	NVM2	NVM1
Power ON Sequence	1'h0	1'h0
S/W Reset	No Change	No Change
H/W Reset	1'h0	1'h0

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4.4.29. LVD Detect (57h)

Page 1 Command Set		57h : LVD (Low Voltage Detection)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	1	1	57h
1st Parameter	Write / Read	0	VDET[2:0]			0	VCORE_VD[2:0]			20h

Description

VCORE_VD[2:0]: Set Vcore voltage adjustment

VCORE_VD[2:0]	Value (V)
000	1.50
001	1.45
010	1.40
011	1.35
100	1.55
101	1.60
110	1.65
111	1.7

VDET[2:0]: Low voltage detection for voltage level setting is defined as below table

VDET[2:0]	Value (V)
000	1.6
001	1.7
010	1.8
011	1.9
100	2.0
101	2.1
110	2.3
111	2.4

Restriction: To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VDET[2:0]	VCORE_VD[2:0]
Power ON Sequence	3’h2	3’h0
S/W Reset	No Change	No Change
H/W Reset	3’h2	3’h0

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4.4.30. Entry Mode Set (58h)

Page 1 Command Set		58h : ETMOD (Entry Mode Set)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	1	0	0	0	58h
1st Parameter	Write / Read	LVD	0	0	1	0	0	0	DSTB	90h

Description

DSTB: The ILI9806E-2C driver enters the Deep Standby Mode when DSTB is set to high (“1”). In Deep Standby mode, when internal logic power is turned off, the structions are not saved. After exiting the Deep Standby Mode , the display pattern and structions need to be rewrited.

The ILI9806E-2C provides two ways to exit Deep Standby Mode:

(1) Exit Deep Standby Mode by pulling down CSX to low (“0”) 6 times.

(2) Input a RESX pulse with effectively low level duration to start up the inside logic regulator and make a transition to the initial state.

Note : See Section 11 Deep Standby Mode Setting

LVD: Low voltage detection control.

LVD	Low voltage detection
0	Disable
1	Enable

Restriction

To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	LVD	DSTB
Power ON Sequence	1’h1	1’h0
S/W Reset	No Change	No Change
H/W Reset	1’h1	1’h0

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4.4.31. Source Timing Adjust 1 (60h)

Page 1 Command Set		60h : Source Timing Adjust 1								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	0	0	60h
1st Parameter	Write / Read	0	0	SDTI[5:0]						05h

Description

SDTI [5:0]: Source SDT timing adjustment (time scale: internal T_{OP_CLK}).

The timing can be adjusted from 0 to 63 time scales.

Note: T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us

Restriction

To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	SDTI[5:0]
Power ON Sequence	6’h05
S/W Reset	No Change
H/W Reset	6’h05

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4.4.32. Source Timing Adjust 2 (61h)

Page 1 Command Set		61h : Source Timing Adjust 2								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	0	1	61h
1st Parameter	Write / Read	0	0	CRTI[5:0]						05h
Description	**CRTI [5:0]**: Source CR timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted from 0 to 63 time scales. Note: T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us									
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CRTI[5:0]
Power ON Sequence	6’h05
S/W Reset	No Change
H/W Reset	6’h05

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4.4.33. Source Timing Adjust 3 (62h)

Page 1 Command Set		62h : Source Timing Adjust 3								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	1	0	62h
1st Parameter	Write / Read	0	0	EQTI[5:0]						0Eh

Description

EQTI [5:0]: Source EQ timing adjustment (time scale: internal T_{OP_CLK}).

The timing can be adjusted from 5 to 63 time scales.

Note: T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us

Restriction

1. To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.
2. The function setting can not be less than 1us.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	EQTI[5:0]
Power ON Sequence	6’h0E
S/W Reset	No Change
H/W Reset	6’h0E

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4.4.34. Source Timing Adjust 4 (63h)

Page 1 Command Set		63h : Source Timing Adjust 4								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	1	0	0	0	1	1	63h
1st Parameter	Write / Read	0	0	PCTI[5:0]						05h
Description	**PCTI [5:0]**: Source PC timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted from 0 to 63 time scales. Note: T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us									
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	PCTI[5:0]
Power ON Sequence	6’h05
S/W Reset	No Change
H/W Reset	6’h05

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4.4.35. Synchronization Timing Adjust 1 (80h)

Page 1 Command Set		80h : Synchronization Time Adjust 1								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	0	0	0	0	0	80h
1st Parameter	Write / Read	TOUCH_OPT[1:0]		VSOD[1:0]		HOSM[1:0]		HS_OPT	0	00h

Description

This command controls the synchronization output .

HS_OPT : Select the output source for HSOUT.

HS_OPT	Description
0	Prebuf-Source
1	HSOUT (Note 2)

HOSM [1:0] : Set the HSOUT active period (time scale: internal T_{OP_CLK}).

HOSM [1:0]		Description
0	0	VACT Period + VFP+VBP
0	1	VACT Period
1	0	VFP+VBP
1	1	Inhibited

VSOD [1:0] : Set the VSOUT timing (time scale: internal T_{OP_CLK}).

VSOD [1:0]		Description
0	0	0 line(First line of back porch)
0	1	1 line
1	0	2 line
1	1	3 line

TOUCH_OPT[1:0] : Select the Output Mode of synchronization (time scale: internal T_{OP_CLK}).

TOUCH_OPT [1:0]		Description
0	0	Off
0	1	VFP+VBP
1	0	Adjustable for VSOUT / HSOUT (Note 2)_
1	1	VFP+VBP / HFP+HBP

Note1 : T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us

Note2 : When use this setting, please reference to Chapter 12.

Restriction

1. To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.
2. When use this function, the data of input must match the resolution thatwas set in Chapter 4.4.12. (P1_ R30h)

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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Default

Status	Default Value			
	TOUCH_OPT [1:0]	VSOD [1:0]	HOSM [1:0]	HS_OPT
Power ON Sequence	2'h0	2'h0	2'h0	1'h0
S/W Reset	No Change	No Change	No Change	No Change
H/W Reset	2'h0	2'h0	2'h0	1'h0

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4.4.36. Synchronization Timing Adjust 2 (81h)

Page 1 Command Set		81h : Synchronization Time Adjust 2								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	0	0	0	0	1	81h
1st Parameter	Write / Read	0	HSOD[6:0]							05h

Description

HSOD [6:0] : Set the HSOUT timing (time scale: internal T_{OP_CLK}).

HSOD[6:0]	Description
7'h00	0clk
7'h01	1clk
7'h02	2clk
:	:
7'h7D	125clk
7'h7E	126clk
7'h7F	127clk

Note1 : T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us

Note2 : When use the setting, please reference to Chapter 12

Restriction

1. To enable this command, "Page 1 Command Set enable register (FFh) " must set first.
2. When use this function, the data of input must match the resolution thatwas set in Chapter 4.4.12. (P1_ R30h)

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	HSOD[6:0]
Power ON Sequence	7'h05
S/W Reset	No Change
H/W Reset	7'h05

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4.4.37. Synchronization Timing Adjust 3 (82h)

Page 1 Command Set		82h : Synchronization Time Adjust 3								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	0	0	0	0	1	0	82h
1st Parameter	Write / Read	HSOHW[7:0]								19h

Description

HSOHW [7:0] : Set the high width of HSOUT (time scale: internal T_{OP_CLK}).

HSOHW[7:0]	Description
8'h00	0clk
8'h01	1clk
8'h02	2clk
:	:
8'hFD	253clk
8'hFE	254clk
8'hFF	255clk

Note1 : T_{OP_CLK} : 4* T_{OSC_CLK} = 0.22us

Note2 : When use the setting, please reference to Chapter 12

Restriction

1. To enable this command, "Page 1 Command Set enable register (FFh) " must set first.
2. When use this function, the data of input must match the resolution thatwas set in Chapter 4.4.12. (P1_ R30h)

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	HSOHW[7:0]
Power ON Sequence	8'h19
S/W Reset	No Change
H/W Reset	8'h19

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4.4.38. Positive Gamma Control 1~16 (A0h~AFh)

Page 1 Command Set										
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
A0h	Write	0	0	REGAM0_P [5:0]						00h
A1h	Write	0	0	REGAM4_P [5:0]						0Fh
A2h	Write	0	0	REGAM8_P [5:0]						19h
A3h	Write	0	0	0	REGAM16_P [4:0]					12h
A4h	Write	0	0	0	REGAM24_P [4:0]					13h
A5h	Write	0	0	0	REGAM52_P [4:0]					1Ah
A6h	Write	0	0	0	0	REGAM80_P [3:0]				0Dh
A7h	Write	0	0	0	0	REGAM108_P [3:0]				0Ch
A8h	Write	0	0	0	0	REGAM147_P [3:0]				00h
A9h	Write	0	0	0	0	REGAM175_P [3:0]				04h
AAh	Write	0	0	0	REGAM203_P [4:0]					04h
ABh	Write	0	0	0	REGAM231_P [4:0]					0Dh
ACh	Write	0	0	0	REGAM239_P [4:0]					0Bh
ADh	Write	0	0	REGAM247_P [5:0]						2Ah
AEh	Write	0	0	REGAM251_P [5:0]						20h
AFh	Write	0	0	REGAM255_P [5:0]						00h
Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.									
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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4.4.39. Negative Gamma Correction 1~16 (C0h~CFh)

Page 1 Command Set										
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
C0h	Write	0	0	REGAM0_N[5:0]						00h
C1h	Write	0	0	REGAM4_N[5:0]						0Fh
C2h	Write	0	0	REGAM8_N [5:0]						19h
C3h	Write	0	0	0	REGAM16_N [4:0]					12h
C4h	Write	0	0	0	REGAM24_N [4:0]					13h
C5h	Write	0	0	0	REGAM52_N [4:0]					1Ah
C6h	Write	0	0	0	0	REGAM80_N[3:0]				0Dh
C7h	Write	0	0	0	0	REGAM108_N [3:0]				0Ch
C8h	Write	0	0	0	0	REGAM147_N [3:0]				00h
C9h	Write	0	0	0	0	REGAM175_N [3:0]				04h
CAh	Write	0	0	0	REGAM203_N [4:0]					04h
CBh	Write	0	0	0	REGAM231_N [4:0]					0Dh
CCh	Write	0	0	0	REGAM239_N [4:0]					0Bh
CDh	Write	0	0	REGAM247_N [5:0]						2Ah
CEh	Write	0	0	REGAM251_N [5:0]						20h
CFh	Write	0	0	REGAM255_N [5:0]						00h

Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.
Register Availability	

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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4.4.40. NV Memory Write1~2 (E0h~ E1h)

Page 1 Command Set		E0h : NVMWR1 (NV Memory Write1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	0	0	E0h
1st Parameter	Write	PGM_DATA [7:0]								00

Page 1 Command Set		E1h : NVMWR2 (NV Memory Write2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	0	1	E1h
1st Parameter	Write	PGM_ADR [7:0] / NVM_READ_ADR [7:0]								00

Description

This command is used to program or read the NV memory data.

After a successful OTP operation, the information of PGM_DATA [7:0] will be programmed to the NV memory.

PGM_DATA [7:0]: The programmed data.

PGM_ADR [7:0] / NVM_READ_ADR [7:0] : Set the address of the NV memory for programming or read data. See "NV Memory Programming flow" and "NV Memory Read flow".

PGM_ADR [7:0]	NVM_READ_ADR [7:0]			Programming data
	1st time	2nd time	3rd time	
8'h01	8'h09	8'h0A	8'h0C	ID1
8'h 02	8'h0D	8'h0E	8'h10	ID2
8'h 03	8'h11	8'h12	8'h14	ID3
8'h 04	8'h15	8'h15	8'h15	VCM1[8]
8'h 05	8'h16	8'h18	8'h19	VCM1[7:0]
8'h 06	8'h15	8'h15	8'h15	VCM2[8]
8'h 07	8'h1A	8'h1C	8'h1D	VCM2[7:0]
8'h 08	8'h1E	8'h20	-	VREG1[7:0]
8'h 09	8'h21	8'h22	-	VREG2[7:0]
8'h 29(Note)	8'h 29	-	-	REGAM0_P
8'h 2A(Note)	8'h 2A	-	-	REGAM4_P
8'h 2C(Note)	8'h 2C	-	-	REGAM8_P
8'h 2D(Note)	8'h 2D	-	-	REGAM16_P
8'h 2E(Note)	8'h 2E	-	-	REGAM24_P
8'h 30(Note)	8'h 30	-	-	REGAM52_P
8'h 31(Note)	8'h 31	-	-	REGAM80_P
8'h 32(Note)	8'h 32	-	-	REGAM108_P
8'h 34(Note)	8'h 34	-	-	REGAM147_P
8'h 35(Note)	8'h 35	-	-	REGAM175_P
8'h 36(Note)	8'h 36	-	-	REGAM203_P
8'h 38(Note)	8'h 38	-	-	REGAM231_P
8'h 39(Note)	8'h 39	-	-	REGAM239_P
8'h 3A(Note)	8'h 3A	-	-	REGAM247_P
8'h 3C(Note)	8'h 3C	-	-	REGAM251_P
8'h 3D(Note)	8'h 3D	-	-	REGAM255_P
8'h 3E(Note)	8'h 3E	-	-	REGAM0_N
8'h 40(Note)	8'h 40	-	-	REGAM4_N
8'h 41(Note)	8'h 41	-	-	REGAM8_N
8'h 42(Note)	8'h 42	-	-	REGAM16_N
8'h 44(Note)	8'h 44	-	-	REGAM24_N
8'h 45(Note)	8'h 45	-	-	REGAM52_N
8'h 46(Note)	8'h 46	-	-	REGAM80_N
8'h 48(Note)	8'h 48	-	-	REGAM108_N
8'h 49(Note)	8'h 49	-	-	REGAM147_N
8'h 4A(Note)	8'h 4A	-	-	REGAM175_N

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	8'h 4C(Note)	8'h 4C	-	-	REGAM203_N
	8'h 4D(Note)	8'h 4D	-	-	REGAM231_N
	8'h 4E(Note)	8'h 4E	-	-	REGAM239_N
	8'h 50(Note)	8'h 50	-	-	REGAM247_N
	8'h 51(Note)	8'h 51	-	-	REGAM251_N
	8'h 52(Note)	8'h 52	-	-	REGAM255_N

Note : The program, REGAM0_P~ REGAM255_P and REGAM0_N~ REGAM255_N, are completed after all addresses must finish.

Restriction	To enable this command, "Page 1 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	PGM_ADR [7:0] / NVM_READ_ADR[7:0]	PGM_DATA [7:0]
Power ON Sequence	8'h00	8'h00
S/W Reset	No change	No change
H/W Reset	8'h00	8'h00

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4.4.41. NV Memory Protection Key1~3 (E3h~ E5h)

Page 1 Command Set		E3h : NVMPKEY1 (NV Memory Protection Key1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	1	1	E3h
1st Parameter	Write	KEY[23:16]								XXh

Page 1 Command Set		E4h : NVMPKEY2 (NV Memory Protection Key2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	1	0	0	E4h
1st Parameter	Write	KEY[15:8]								XXh

Page 1 Command Set		E5h : NVMPKEY3 (NV Memory Protection Key3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	1	0	1	E5h
1st Parameter	Write	KEY[7:0]								XXh
Description	**KEY [23:0]:** NV memory programming protection key. Write an OTP data to E0h, this KEY[23:0] must set 0x55AA66h to enable OTP programming, And set 0x116688h to enable OTP read. If the KEY[23:0] is not 0x55AA66h and 0x116688h, the NV Memory program will be failed.									
Restriction	To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power ON Sequence	24’h000000
S/W Reset	24’h000000

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4.4.42. NV Memory Status Read1 (E6h)

Page 1 Command Set		E6h : RDNVM1 (NV Memory Status Read1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	1	1	0	E6h
1st Parameter	Read	0	0	ID2_ MK [2:0]			ID1_ MK [2:0]			00h

Description

The register uses a mark to record the NV memory programmed time. The bits are increase "+1" automatically after writing the PGM_DATA [7:0] to the NV memory.

ID1_MK [2:0]/ID2_MK [2:0]:

ID1_ MK [2:0]/ID2_MK [2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

Restriction

To enable this command, "Page 1 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	ID2_ MK [2:0]	ID1_ MK [2:0]
Power ON Sequence	3'h0	3'h0
S/W Reset	3'h0	3'h0

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4.4.43. NV Memory Status Read2 (E7h)

<table>
<tr><th colspan="2">Page 1 Command Set</th><th colspan="9">E7h : RDNVM2 (NV Memory Status Read2)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>E7h</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">ID3_ MK [2:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">The register uses a mark to record the NV memory programmed time. The bits are increase “+1” automatically after writing the PGM_DATA [7:0] to the NV memory.
ID3_MK [2:0]:
<table>
<tr><th colspan="3">ID3_MK [2:0]</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No Programmed</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Programmed 1 time already</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Programmed 2 times already</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Programmed 3 times already</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 1 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>ID3_ MK [2:0]</th></tr>
<tr><td>Power ON Sequence</td><td>3’h0</td></tr>
<tr><td>S/W Reset</td><td>3’h0</td></tr>
</table></td></tr>
</table>

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4.4.44. NV Memory Status Read3 (E8h)

Page 1 Command Set		E8h : RDNVM3 (NV Memory Status Read3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	1	0	0	0	E8h
1st Parameter	Read	GMAP_MK	GMAN_MK	VCM2_MK [2:0]			VCM1_MK [2:0]			00h

Description

The register uses a mark to record the NV memory programmed time. The bits are increase "+1" automatically after writing the PGM_DATA [7:0] to the NV memory.

VCM1_MK [2:0] /VCM2_MK [2:0]:

VCM1_MK [2:0] /VCM2_MK [2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

GAMP_MK / GAMN_MK :

GAMP_MK / GAMN_MK	Description
0	No Programmed
1	Programmed 1 time already

Restriction

To enable this command, "Page 1 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	GAMP_MK	GAMN_MK	VCM2_MK [2:0]	VCM1_MK [2:0]
Power ON Sequence	1'h0	1'h0	3'h0	3'h0
S/W Reset	1'h0	1'h0	3'h0	3'h0

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4.4.45. NV Memory Status Read4 (E9h)

Page 1 Command Set		E9h : RDNVM4 (NV Memory Status Read4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	1	0	0	1	E9h
1st Parameter	Read	OTP BUSY	0	0	0	0	0	0	0	00h
Description	The register uses a mark to record the NV memory programmed time. The bits are increase "+1" automatically after writing the PGM_DATA [7:0] to the NV memory. **OTP BUSY:** The status bit of the NV memory programming.									
Restriction	To enable this command, "Page 1 Command Set enable register (FFh) " must set first.									
Register Availability										
Default										

BUSY	The Status of NV Memory
0	Idle
1	Busy

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
	OTP BUSY
Power ON Sequence	1'h0
S/W Reset	1'h0

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4.4.46. NV Memory Status Read5 (EAh)

Page 1 Command Set		EAh : RDNVM5 (NV Memory Status Read5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	1	0	1	0	EAh
1st Parameter	Read	NVM_READ_DATA [7:0]								XXh
Description	**NVM_READ_DATA[7:0]:** The NV memory data of the "NVM_READ_ADR[7:0]" address is read out. See figure "NV Memory Read flow"..									
Restriction	To enable this command, "Page 1 Command Set enable register (FFh) " must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	NVM_READ_DATA [7:0]
Power ON Sequence	8'h00
S/W Reset	8'h00

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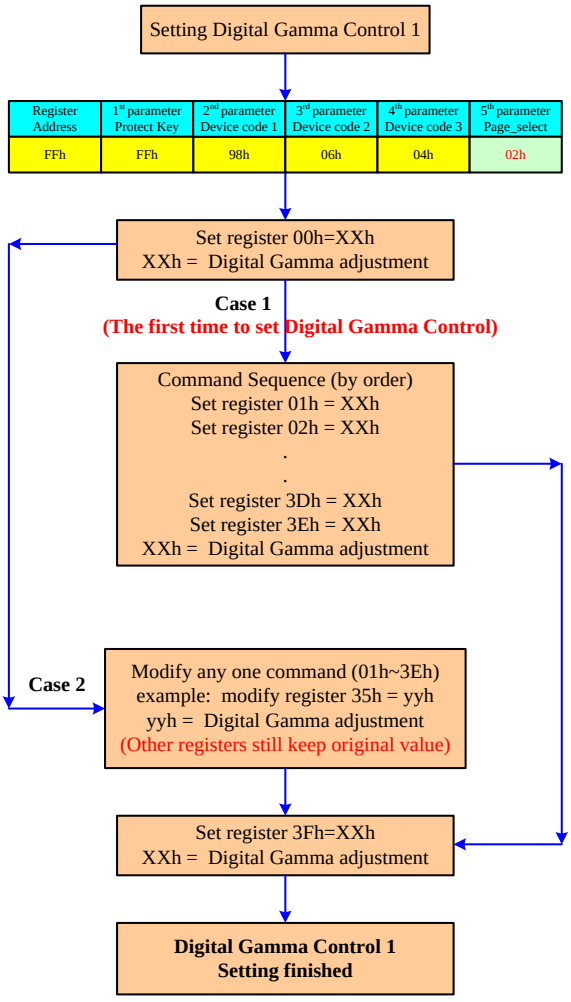
4.5. Page 2 Command Description

4.5.1. Digital Gamma Control 1 (00h~3Fh)

Page 2 Command Set										
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write	RCA0 [3:0]				BCA0 [3:0]				-
01h	Write	RCA1 [3:0]				BCA1 [3:0]				-
02h	Write	RCA2 [3:0]				BCA2 [3:0]				-
03h	Write	RCA3 [3:0]				BCA3 [3:0]				-
04h	Write	RCA4 [3:0]				BCA4 [3:0]				-
05h	Write	RCA5 [3:0]				BCA5 [3:0]				-
06h	Write	RCA6 [3:0]				BCA6 [3:0]				-
07h	Write	RCA7 [3:0]				BCA7 [3:0]				-
08h	Write	RCA8 [3:0]				BCA8 [3:0]				-
09h	Write	RCA9 [3:0]				BCA9 [3:0]				-
0Ah	Write	RCA10 [3:0]				BCA10 [3:0]				-
0Bh	Write	RCA11 [3:0]				BCA11 [3:0]				-
0Ch	Write	RCA12 [3:0]				BCA12 [3:0]				-
0Dh	Write	RCA13 [3:0]				BCA13 [3:0]				-
0Eh	Write	RCA14 [3:0]				BCA14 [3:0]				-
0Fh	Write	RCA15 [3:0]				BCA15 [3:0]				-
10h	Write	RCA16 [3:0]				BCA16 [3:0]				-
11h	Write	RCA17 [3:0]				BCA17 [3:0]				-
12h	Write	RCA18 [3:0]				BCA18 [3:0]				-
13h	Write	RCA19 [3:0]				BCA19 [3:0]				-
14h	Write	RCA20 [3:0]				BCA20 [3:0]				-
15h	Write	RCA21 [3:0]				BCA21 [3:0]				-
16h	Write	RCA22 [3:0]				BCA22 [3:0]				-
17h	Write	RCA23 [3:0]				BCA23 [3:0]				-
18h	Write	RCA24 [3:0]				BCA24 [3:0]				-
19h	Write	RCA25 [3:0]				BCA25 [3:0]				-
1Ah	Write	RCA26 [3:0]				BCA26 [3:0]				-
1Bh	Write	RCA27 [3:0]				BCA27 [3:0]				-
1Ch	Write	RCA28 [3:0]				BCA28 [3:0]				-
1Dh	Write	RCA29 [3:0]				BCA29 [3:0]				-
1Eh	Write	RCA30 [3:0]				BCA30 [3:0]				-
1Fh	Write	RCA31 [3:0]				BCA31 [3:0]				-
20h	Write	RCA32 [3:0]				BCA32 [3:0]				-
21h	Write	RCA33 [3:0]				BCA33 [3:0]				-
22h	Write	RCA34 [3:0]				BCA34 [3:0]				-
23h	Write	RCA35 [3:0]				BCA35 [3:0]				-
24h	Write	RCA36 [3:0]				BCA36 [3:0]				-
25h	Write	RCA37 [3:0]				BCA37 [3:0]				-
26h	Write	RCA38 [3:0]				BCA38 [3:0]				-
27h	Write	RCA39 [3:0]				BCA39 [3:0]				-
28h	Write	RCA40 [3:0]				BCA40 [3:0]				-
29h	Write	RCA41 [3:0]				BCA41 [3:0]				-
2Ah	Write	RCA42 [3:0]				BCA42 [3:0]				-
2Bh	Write	RCA43 [3:0]				BCA43 [3:0]				-
2Ch	Write	RCA44 [3:0]				BCA44 [3:0]				-
2Dh	Write	RCA45 [3:0]				BCA45 [3:0]				-
2Eh	Write	RCA46 [3:0]				BCA46 [3:0]				-
2Fh	Write	RCA47 [3:0]				BCA47 [3:0]				-
30h	Write	RCA48 [3:0]				BCA48 [3:0]				-

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31h	Write	RCA49 [3:0]	BCA49 [3:0]	-
32h	Write	RCA50 [3:0]	BCA50 [3:0]	-
33h	Write	RCA51 [3:0]	BCA51 [3:0]	-
34h	Write	RCA52 [3:0]	BCA52 [3:0]	-
35h	Write	RCA53 [3:0]	BCA53 [3:0]	-
36h	Write	RCA54 [3:0]	BCA54 [3:0]	-
37h	Write	RCA55 [3:0]	BCA55 [3:0]	-
38h	Write	RCA56 [3:0]	BCA56 [3:0]	-
39h	Write	RCA57 [3:0]	BCA57 [3:0]	-
3Ah	Write	RCA58 [3:0]	BCA58 [3:0]	-
3Bh	Write	RCA59 [3:0]	BCA59 [3:0]	-
3Ch	Write	RCA60 [3:0]	BCA60 [3:0]	-
3Dh	Write	RCA61 [3:0]	BCA61 [3:0]	-
3Eh	Write	RCA62 [3:0]	BCA62 [3:0]	-
3Fh	Write	RCA63 [3:0]	BCA63 [3:0]	-
Description	**RCAx [3:0]:** Gamma Macro-adjustment registers for red Gamma curve. **BCAx [3:0]:** Gamma Macro-adjustment registers for blue Gamma curve.			
Restriction	To enable this command, “Page 2 Command Set enable register (FFh) ” must set first.			



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Register Availability	

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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4.5.2. Digital 3 Gamma Enable (40h)

Page 2 Command Set		40h : D3GE (Digital 3 Gamma Enable)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	0	0	0	0	0	40h
1st Parameter	Write / Read	0	0	0	0	0	0	0	En_3G	00h
Description	**En_3G:** 0 : digital 3 gamma disable 1 : digital 3 gamma enable									
Restriction	To enable this command, “Page 2 Command Set enable register (FFh) ” must set first.									
Register Availability										

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	En_3G
Power ON Sequence	1’h0
S/W Reset	No change
H/W Reset	1’h0

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4.6. Page 3 Command Description

4.6.1. Digital Gamma Control 2 (00h~7Fh)

Page 3 Command Set									
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write	RFA0 [3:0]				BFA0 [3:0]				-
01h	Write	RFA1 [3:0]				BFA1 [3:0]				-
02h	Write	RFA2 [3:0]				BFA2 [3:0]				-
03h	Write	RFA3 [3:0]				BFA3 [3:0]				-
04h	Write	RFA4 [3:0]				BFA4 [3:0]				-
05h	Write	RFA5 [3:0]				BFA5 [3:0]				-
06h	Write	RFA6 [3:0]				BFA6 [3:0]				-
07h	Write	RFA7 [3:0]				BFA7 [3:0]				-
08h	Write	RFA8 [3:0]				BFA8 [3:0]				-
09h	Write	RFA9 [3:0]				BFA9 [3:0]				-
0Ah	Write	RFA10 [3:0]				BFA10 [3:0]				-
0Bh	Write	RFA11 [3:0]				BFA11 [3:0]				-
0Ch	Write	RFA12 [3:0]				BFA12 [3:0]				-
0Dh	Write	RFA13 [3:0]				BFA13 [3:0]				-
0Eh	Write	RFA14 [3:0]				BFA14 [3:0]				-
0Fh	Write	RFA15 [3:0]				BFA15 [3:0]				-
10h	Write	RFA16 [3:0]				BFA16 [3:0]				-
11h	Write	RFA17 [3:0]				BFA17 [3:0]				-
12h	Write	RFA18 [3:0]				BFA18 [3:0]				-
13h	Write	RFA19 [3:0]				BFA19 [3:0]				-
14h	Write	RFA20 [3:0]				BFA20 [3:0]				-
15h	Write	RFA21 [3:0]				BFA21 [3:0]				-
16h	Write	RFA22 [3:0]				BFA22 [3:0]				-
17h	Write	RFA23 [3:0]				BFA23 [3:0]				-
18h	Write	RFA24 [3:0]				BFA24 [3:0]				-
19h	Write	RFA25 [3:0]				BFA25 [3:0]				-
1Ah	Write	RFA26 [3:0]				BFA26 [3:0]				-
1Bh	Write	RFA27 [3:0]				BFA27 [3:0]				-
1Ch	Write	RFA28 [3:0]				BFA28 [3:0]				-
1Dh	Write	RFA29 [3:0]				BFA29 [3:0]				-
1Eh	Write	RFA30 [3:0]				BFA30 [3:0]				-
1Fh	Write	RFA31 [3:0]				BFA31 [3:0]				-
20h	Write	RFA32 [3:0]				BFA32 [3:0]				-
21h	Write	RFA33 [3:0]				BFA33 [3:0]				-
22h	Write	RFA34 [3:0]				BFA34 [3:0]				-
23h	Write	RFA35 [3:0]				BFA35 [3:0]				-
24h	Write	RFA36 [3:0]				BFA36 [3:0]				-
25h	Write	RFA37 [3:0]				BFA37 [3:0]				-
26h	Write	RFA38 [3:0]				BFA38 [3:0]				-
27h	Write	RFA39 [3:0]				BFA39 [3:0]				-
28h	Write	RFA40 [3:0]				BFA40 [3:0]				-
29h	Write	RFA41 [3:0]				BFA41 [3:0]				-
2Ah	Write	RFA42 [3:0]				BFA42 [3:0]				-
2Bh	Write	RFA43 [3:0]				BFA43 [3:0]				-
2Ch	Write	RFA44 [3:0]				BFA44 [3:0]				-
2Dh	Write	RFA45 [3:0]				BFA45 [3:0]				-
2Eh	Write	RFA46 [3:0]				BFA46 [3:0]				-
2Fh	Write	RFA47 [3:0]				BFA47 [3:0]				-
30h	Write	RFA48 [3:0]				BFA48 [3:0]				-

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31h	Write	RFA49 [3:0]	BFA49 [3:0]	-
32h	Write	RFA50 [3:0]	BFA50 [3:0]	-
33h	Write	RFA51 [3:0]	BFA51 [3:0]	-
34h	Write	RFA52 [3:0]	BFA52 [3:0]	-
35h	Write	RFA53 [3:0]	BFA53 [3:0]	-
36h	Write	RFA54 [3:0]	BFA54 [3:0]	-
37h	Write	RFA55 [3:0]	BFA55 [3:0]	-
38h	Write	RFA56 [3:0]	BFA56 [3:0]	-
39h	Write	RFA57 [3:0]	BFA57 [3:0]	-
3Ah	Write	RFA58 [3:0]	BFA58 [3:0]	-
3Bh	Write	RFA59 [3:0]	BFA59 [3:0]	-
3Ch	Write	RFA60 [3:0]	BFA60 [3:0]	-
3Dh	Write	RFA61 [3:0]	BFA61 [3:0]	-
3Eh	Write	RFA62 [3:0]	BFA62 [3:0]	-
3Fh	Write	RFA63 [3:0]	BFA63 [3:0]	-
40h	Write	RFA64 [3:0]	BFA64 [3:0]	-
41h	Write	RFA65 [3:0]	BFA65 [3:0]	-
42h	Write	RFA66 [3:0]	BFA66 [3:0]	-
43h	Write	RFA67 [3:0]	BFA67 [3:0]	-
44h	Write	RFA68 [3:0]	BFA68 [3:0]	-
45h	Write	RFA69 [3:0]	BFA69 [3:0]	-
46h	Write	RFA70 [3:0]	BFA70 [3:0]	-
47h	Write	RFA71 [3:0]	BFA71 [3:0]	-
48h	Write	RFA72 [3:0]	BFA72 [3:0]	-
49h	Write	RFA73 [3:0]	BFA73 [3:0]	-
4Ah	Write	RFA74 [3:0]	BFA74 [3:0]	-
4Bh	Write	RFA75 [3:0]	BFA75 [3:0]	-
4Ch	Write	RFA76 [3:0]	BFA76 [3:0]	-
4Dh	Write	RFA77 [3:0]	BFA77 [3:0]	-
4Eh	Write	RFA78 [3:0]	BFA78 [3:0]	-
4Fh	Write	RFA79 [3:0]	BFA79 [3:0]	-
50h	Write	RFA80 [3:0]	BFA80 [3:0]	-
51h	Write	RFA81 [3:0]	BFA81 [3:0]	-
52h	Write	RFA82 [3:0]	BFA82 [3:0]	-
53h	Write	RFA83 [3:0]	BFA83 [3:0]	-
54h	Write	RFA84 [3:0]	BFA84 [3:0]	-
55h	Write	RFA85 [3:0]	BFA85 [3:0]	-
56h	Write	RFA86 [3:0]	BFA86 [3:0]	-
57h	Write	RFA87 [3:0]	BFA87 [3:0]	-
58h	Write	RFA88 [3:0]	BFA88 [3:0]	-
59h	Write	RFA89 [3:0]	BFA89 [3:0]	-
5Ah	Write	RFA90 [3:0]	BFA90 [3:0]	-
5Bh	Write	RFA91 [3:0]	BFA91 [3:0]	-
5Ch	Write	RFA92 [3:0]	BFA92 [3:0]	-
5Dh	Write	RFA93 [3:0]	BFA93 [3:0]	-
5Eh	Write	RFA94 [3:0]	BFA94 [3:0]	-
5Fh	Write	RFA95 [3:0]	BFA95 [3:0]	-
60h	Write	RFA96 [3:0]	BFA96 [3:0]	-
61h	Write	RFA97 [3:0]	BFA97 [3:0]	-
62h	Write	RFA98 [3:0]	BFA98 [3:0]	-
63h	Write	RFA99 [3:0]	BFA99 [3:0]	-
64h	Write	RFA100 [3:0]	BFA100 [3:0]	-
65h	Write	RFA101 [3:0]	BFA101 [3:0]	-
66h	Write	RFA102 [3:0]	BFA102 [3:0]	-
67h	Write	RFA103 [3:0]	BFA103 [3:0]	-

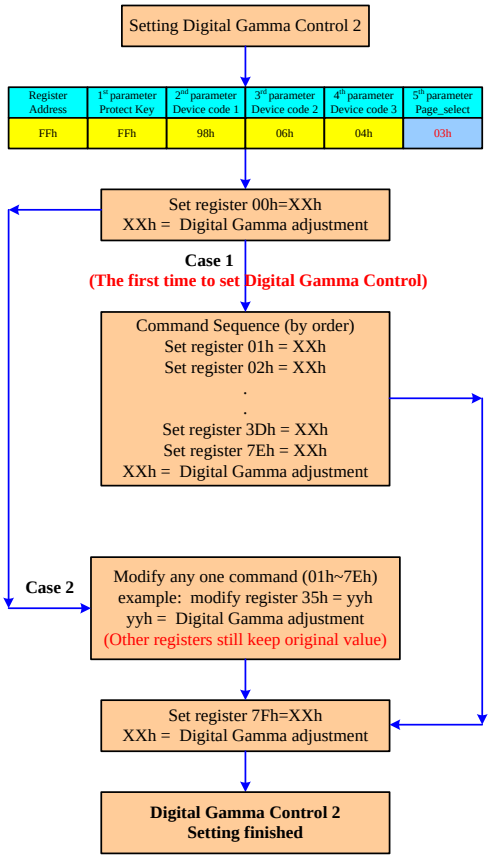
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68h	Write	RFA104 [3:0]	BFA104 [3:0]	-
69h	Write	RFA105 [3:0]	BFA105 [3:0]	-
6Ah	Write	RFA106 [3:0]	BFA106 [3:0]	-
6Bh	Write	RFA107 [3:0]	BFA107 [3:0]	-
6Ch	Write	RFA108 [3:0]	BFA108 [3:0]	-
6Dh	Write	RFA109 [3:0]	BFA109 [3:0]	-
6Eh	Write	RFA110 [3:0]	BFA110 [3:0]	-
6Fh	Write	RFA111 [3:0]	BFA111 [3:0]	-
70h	Write	RFA112 [3:0]	BFA112 [3:0]	-
71h	Write	RFA113 [3:0]	BFA113 [3:0]	-
72h	Write	RFA114 [3:0]	BFA114 [3:0]	-
73h	Write	RFA115 [3:0]	BFA115 [3:0]	-
74h	Write	RFA116 [3:0]	BFA116 [3:0]	-
75h	Write	RFA117 [3:0]	BFA117 [3:0]	-
76h	Write	RFA118 [3:0]	BFA118 [3:0]	-
77h	Write	RFA119 [3:0]	BFA119 [3:0]	-
78h	Write	RFA120 [3:0]	BFA120 [3:0]	-
79h	Write	RFA121 [3:0]	BFA121 [3:0]	-
7Ah	Write	RFA122 [3:0]	BFA122 [3:0]	-
7Bh	Write	RFA123 [3:0]	BFA123 [3:0]	-
7Ch	Write	RFA124 [3:0]	BFA124 [3:0]	-
7Dh	Write	RFA125 [3:0]	BFA125 [3:0]	-
7Eh	Write	RFA126 [3:0]	BFA126 [3:0]	-
7Fh	Write	RFA127 [3:0]	BFA127 [3:0]	-

Description

RFAx [3:0]: Gamma Micro-adjustment register for red Gamma curve.

BFAx [3:0]: Gamma Micro-adjustment register for blue Gamma curve.



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<table>
<tr><td>Restriction</td><td>To enable this command, “Page 3 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

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4.7. Page 4 Command Description

4.7.1. Digital Gamma Control 3 (00h~7Fh)

Page 4 Command Set									
Command	Write / Read	Parameter							Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write	RFA128 [3:0]				BFA128 [3:0]				-
01h	Write	RFA129 [3:0]				BFA129 [3:0]				-
02h	Write	RFA130 [3:0]				BFA130 [3:0]				-
03h	Write	RFA131 [3:0]				BFA131 [3:0]				-
04h	Write	RFA132 [3:0]				BFA132 [3:0]				-
05h	Write	RFA133 [3:0]				BFA133 [3:0]				-
06h	Write	RFA134 [3:0]				BFA134 [3:0]				-
07h	Write	RFA135 [3:0]				BFA135 [3:0]				-
08h	Write	RFA136 [3:0]				BFA136 [3:0]				-
09h	Write	RFA137 [3:0]				BFA137 [3:0]				-
0Ah	Write	RFA138 [3:0]				BFA138 [3:0]				-
0Bh	Write	RFA139 [3:0]				BFA139 [3:0]				-
0Ch	Write	RFA140 [3:0]				BFA140 [3:0]				-
0Dh	Write	RFA141 [3:0]				BFA141 [3:0]				-
0Eh	Write	RFA142 [3:0]				BFA142 [3:0]				-
0Fh	Write	RFA143 [3:0]				BFA143 [3:0]				-
10h	Write	RFA144 [3:0]				BFA144 [3:0]				-
11h	Write	RFA145 [3:0]				BFA145 [3:0]				-
12h	Write	RFA146 [3:0]				BFA146 [3:0]				-
13h	Write	RFA147 [3:0]				BFA147 [3:0]				-
14h	Write	RFA148 [3:0]				BFA148 [3:0]				-
15h	Write	RFA149 [3:0]				BFA149 [3:0]				-
16h	Write	RFA150 [3:0]				BFA150 [3:0]				-
17h	Write	RFA151 [3:0]				BFA151 [3:0]				-
18h	Write	RFA152 [3:0]				BFA152 [3:0]				-
19h	Write	RFA153 [3:0]				BFA153 [3:0]				-
1Ah	Write	RFA154 [3:0]				BFA154 [3:0]				-
1Bh	Write	RFA155 [3:0]				BFA155 [3:0]				-
1Ch	Write	RFA156 [3:0]				BFA156 [3:0]				-
1Dh	Write	RFA157 [3:0]				BFA157 [3:0]				-
1Eh	Write	RFA158 [3:0]				BFA158 [3:0]				-
1Fh	Write	RFA159 [3:0]				BFA159 [3:0]				-
20h	Write	RFA160 [3:0]				BFA160 [3:0]				-
21h	Write	RFA161 [3:0]				BFA161 [3:0]				-
22h	Write	RFA162 [3:0]				BFA162 [3:0]				-
23h	Write	RFA163 [3:0]				BFA163 [3:0]				-
24h	Write	RFA164 [3:0]				BFA164 [3:0]				-
25h	Write	RFA165 [3:0]				BFA165 [3:0]				-
26h	Write	RFA166 [3:0]				BFA166 [3:0]				-
27h	Write	RFA167 [3:0]				BFA167 [3:0]				-
28h	Write	RFA168 [3:0]				BFA168 [3:0]				-
29h	Write	RFA169 [3:0]				BFA169 [3:0]				-
2Ah	Write	RFA170 [3:0]				BFA170 [3:0]				-
2Bh	Write	RFA171 [3:0]				BFA171 [3:0]				-
2Ch	Write	RFA172 [3:0]				BFA172 [3:0]				-
2Dh	Write	RFA173 [3:0]				BFA173 [3:0]				-
2Eh	Write	RFA174 [3:0]				BFA174 [3:0]				-
2Fh	Write	RFA175 [3:0]				BFA175 [3:0]				-
30h	Write	RFA176 [3:0]				BFA176 [3:0]				-

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31h	Write	RFA177 [3:0]	BFA177 [3:0]	-
32h	Write	RFA178 [3:0]	BFA178 [3:0]	-
33h	Write	RFA179 [3:0]	BFA179 [3:0]	-
34h	Write	RFA180 [3:0]	BFA180 [3:0]	-
35h	Write	RFA181 [3:0]	BFA181 [3:0]	-
36h	Write	RFA182 [3:0]	BFA182 [3:0]	-
37h	Write	RFA183 [3:0]	BFA183 [3:0]	-
38h	Write	RFA184 [3:0]	BFA184 [3:0]	-
39h	Write	RFA185 [3:0]	BFA185 [3:0]	-
3Ah	Write	RFA186 [3:0]	BFA186 [3:0]	-
3Bh	Write	RFA187 [3:0]	BFA187 [3:0]	-
3Ch	Write	RFA188 [3:0]	BFA188 [3:0]	-
3Dh	Write	RFA189 [3:0]	BFA189 [3:0]	-
3Eh	Write	RFA190 [3:0]	BFA190 [3:0]	-
3Fh	Write	RFA191 [3:0]	BFA191 [3:0]	-
40h	Write	RFA192 [3:0]	BFA192 [3:0]	-
41h	Write	RFA193 [3:0]	BFA193 [3:0]	-
42h	Write	RFA194 [3:0]	BFA194 [3:0]	-
43h	Write	RFA195 [3:0]	BFA195 [3:0]	-
44h	Write	RFA196 [3:0]	BFA196 [3:0]	-
45h	Write	RFA197 [3:0]	BFA197 [3:0]	-
46h	Write	RFA198 [3:0]	BFA198 [3:0]	-
47h	Write	RFA199 [3:0]	BFA199 [3:0]	-
48h	Write	RFA200 [3:0]	BFA200 [3:0]	-
49h	Write	RFA201 [3:0]	BFA201 [3:0]	-
4Ah	Write	RFA202 [3:0]	BFA202 [3:0]	-
4Bh	Write	RFA203 [3:0]	BFA203 [3:0]	-
4Ch	Write	RFA204 [3:0]	BFA204 [3:0]	-
4Dh	Write	RFA205 [3:0]	BFA205 [3:0]	-
4Eh	Write	RFA206 [3:0]	BFA206 [3:0]	-
4Fh	Write	RFA207 [3:0]	BFA207 [3:0]	-
50h	Write	RFA208 [3:0]	BFA208 [3:0]	-
51h	Write	RFA209 [3:0]	BFA209 [3:0]	-
52h	Write	RFA210 [3:0]	BFA210 [3:0]	-
53h	Write	RFA211 [3:0]	BFA211 [3:0]	-
54h	Write	RFA212 [3:0]	BFA212 [3:0]	-
55h	Write	RFA213 [3:0]	BFA213 [3:0]	-
56h	Write	RFA214 [3:0]	BFA214 [3:0]	-
57h	Write	RFA215 [3:0]	BFA215 [3:0]	-
58h	Write	RFA216 [3:0]	BFA216 [3:0]	-
59h	Write	RFA217 [3:0]	BFA217 [3:0]	-
5Ah	Write	RFA218 [3:0]	BFA218 [3:0]	-
5Bh	Write	RFA219 [3:0]	BFA219 [3:0]	-
5Ch	Write	RFA220 [3:0]	BFA220 [3:0]	-
5Dh	Write	RFA221 [3:0]	BFA221 [3:0]	-
5Eh	Write	RFA222 [3:0]	BFA222 [3:0]	-
5Fh	Write	RFA223 [3:0]	BFA223 [3:0]	-
60h	Write	RFA224 [3:0]	BFA224 [3:0]	-
61h	Write	RFA225 [3:0]	BFA225 [3:0]	-
62h	Write	RFA226 [3:0]	BFA226 [3:0]	-
63h	Write	RFA227 [3:0]	BFA227 [3:0]	-
64h	Write	RFA228 [3:0]	BFA228 [3:0]	-
65h	Write	RFA229 [3:0]	BFA229 [3:0]	-
66h	Write	RFA230 [3:0]	BFA230 [3:0]	-
67h	Write	RFA231 [3:0]	BFA231 [3:0]	-

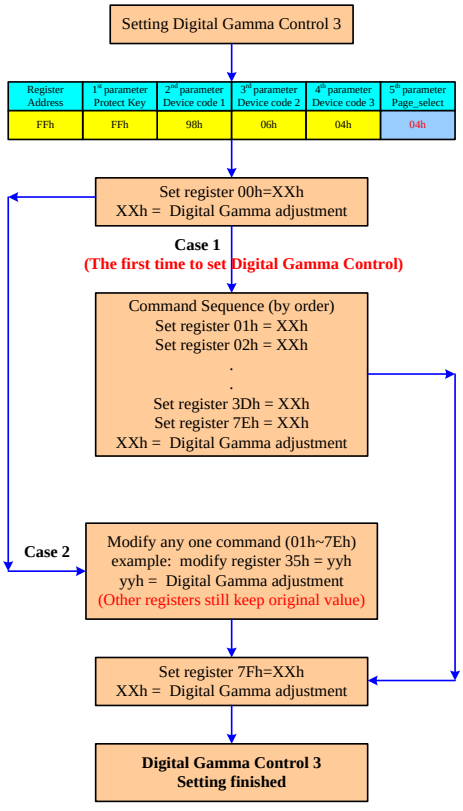
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68h	Write	RFA232 [3:0]	BFA232 [3:0]	-
69h	Write	RFA233 [3:0]	BFA233 [3:0]	-
6Ah	Write	RFA234 [3:0]	BFA234 [3:0]	-
6Bh	Write	RFA235 [3:0]	BFA235 [3:0]	-
6Ch	Write	RFA236 [3:0]	BFA236 [3:0]	-
6Dh	Write	RFA237 [3:0]	BFA237 [3:0]	-
6Eh	Write	RFA238 [3:0]	BFA238 [3:0]	-
6Fh	Write	RFA239 [3:0]	BFA239 [3:0]	-
70h	Write	RFA240 [3:0]	BFA240 [3:0]	-
71h	Write	RFA241 [3:0]	BFA241 [3:0]	-
72h	Write	RFA242 [3:0]	BFA242 [3:0]	-
73h	Write	RFA243 [3:0]	BFA243 [3:0]	-
74h	Write	RFA244 [3:0]	BFA244 [3:0]	-
75h	Write	RFA245 [3:0]	BFA245 [3:0]	-
76h	Write	RFA246 [3:0]	BFA246 [3:0]	-
77h	Write	RFA247 [3:0]	BFA247 [3:0]	-
78h	Write	RFA248 [3:0]	BFA248 [3:0]	-
79h	Write	RFA249 [3:0]	BFA249 [3:0]	-
7Ah	Write	RFA250 [3:0]	BFA250 [3:0]	-
7Bh	Write	RFA251 [3:0]	BFA251 [3:0]	-
7Ch	Write	RFA252 [3:0]	BFA252 [3:0]	-
7Dh	Write	RFA253 [3:0]	BFA253 [3:0]	-
7Eh	Write	RFA254 [3:0]	BFA254 [3:0]	-
7Fh	Write	RFA255 [3:0]	BFA255 [3:0]	-

Description

RFAx [3:0]: Gamma Micro-adjustment register for red Gamma curve.

BFAx [3:0]: Gamma Micro-adjustment register for blue Gamma curve.



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<table>
<tr><td>Restriction</td><td>To enable this command, “Page 4 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

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4.8. Page 5 Command Description

4.8.1. Backlight Control 1 (00h)

Page 5 Command Set		00h : BLCTRL1 (Backlight Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	Write / Read	PWM_DIV[7:0]								E8h

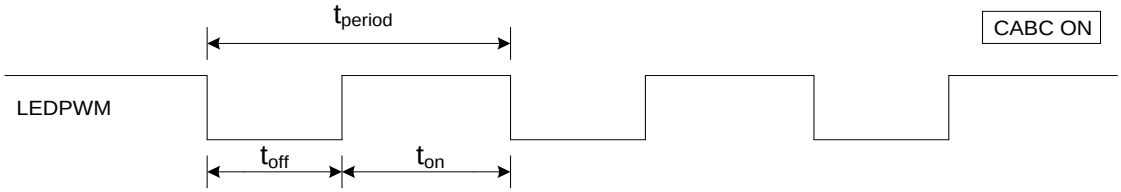
Description

PWM_DIV [7:0]: LEDPWM output period control. This command is used to adjust the PWM waveform period of LEDPWM.

The PWM period is calculated by using the following equation.

$$f_{LEDPWM} = \frac{18MHz}{(PWM_DIV[7:0]+1)\times 255}$$

PWM_DIV[7:0								F_{LEDPWM}
D7	D6	D	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	70.58 KHz
0	0	0	0	0	0	0	1	35.29 KHz
0	0	0	0	0	0	1	0	23.53 KHz
0	0	0	0	0	0	1	1	17.65 KHz
0	0	0	0	0	1	0	0	14.12 KHz
:								:
1	1	1	1	1	0	1	1	280.1 Hz
1	1	1	1	1	1	0	0	279.0 Hz
1	1	1	1	1	1	0	1	277.9 Hz
1	1	1	1	1	1	1	0	276.8 Hz
1	1	1	1	1	1	1	1	275.7 Hz



Note : The output frequency tolerance of internal frequency divider in CABC is ±10%

Restriction

To enable this command, “Page 5 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	PWM_DIV[7:0]
Power ON Sequence	8’hE8
S/W Reset	No change
H/W Reset	8’hE8

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4.8.2. Backlight Control 2 (01h)

Page 5 Command Set		01h : BLCTRL2 (Backlight Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	1	01h
1st Parameter	Write / Read	THRES_MOV[3:0]				THRES_STILL[3:0]				BBh

Description

THRES_MOV [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total number of pixels by image process in Moving Image mode. After this parameter sets the number of pixels that makes display image white, then the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

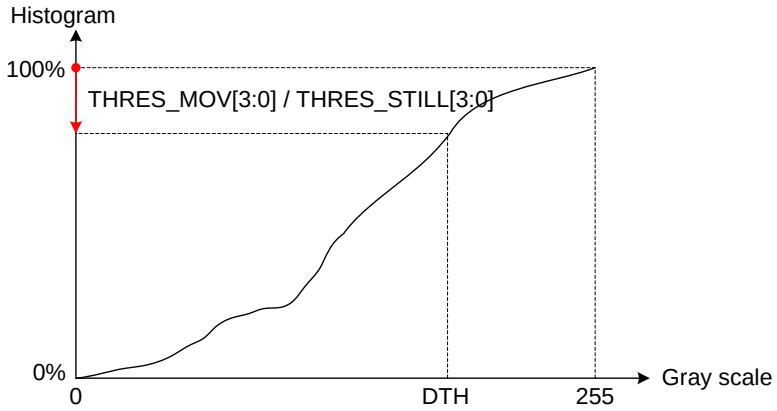
THRES_MOV[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_MOV[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %

THRES_STILL [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total number of pixels by image process in Still Picture mode. After this parameter sets the number of pixels that makes display image white, then the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_STILL[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_STILL[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



Restriction: To enable this command, "Page 5 Command Set enable register (FFh) " must set first.

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Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	THRES_MOV[3:0]	THRES_STILL[3:0]
Power ON Sequence	4'hB	4'hB
S/W Reset	No change	No change
H/W Reset	4'hB	4'hB

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4.8.3. Backlight Control 3 (02h)

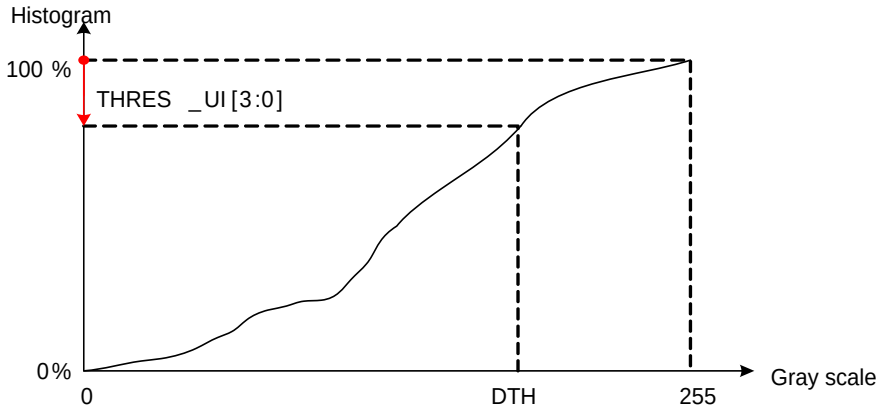
Page 5 Command Set		02h : BLCTRL3 (Backlight Control 3)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	0	02h
1st Parameter	Write / Read	0	0	0	0	THRES_UI[3:0]				0Bh

Description

THRES_UI [3:0]: This parameter is used to set the ratio (percentage) of the maximum number of pixels that makes display image white (data="63) to the total number of pixels by image process in UI (User Interface Image mode). After this parameter sets the number of pixels that makes display image white, then the threshold grayscale value (DTH) that makes display image white is set so that the number of the pixels set by this parameter does not change.

THRES_UI[3:0]				Description
D3	D2	D1	D0	
0	0	0	0	99 %
0	0	0	1	98 %
0	0	1	0	96 %
0	0	1	1	94 %
0	1	0	0	92 %
0	1	0	1	90 %
0	1	1	0	88 %
0	1	1	1	86 %

THRES_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	84 %
1	0	0	1	82 %
1	0	1	0	80 %
1	0	1	1	78 %
1	1	0	0	76 %
1	1	0	1	74 %
1	1	1	0	72 %
1	1	1	1	70 %



Restriction: To enable this command, "Page 5 Command Set enable register (FFh) " must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	THRES_UI
Power ON Sequence	4'hB
S/W Reset	No change
H/W Reset	4'hB

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4.8.4. Backlight Control 4 (03h)

Page 5 Command Set		03h : BLCTRL4 (Backlight Control 4)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	1	03h
1st Parameter	Write / Read	DTH_MOV[3:0]				DTH_STILL[3:0]				A8h

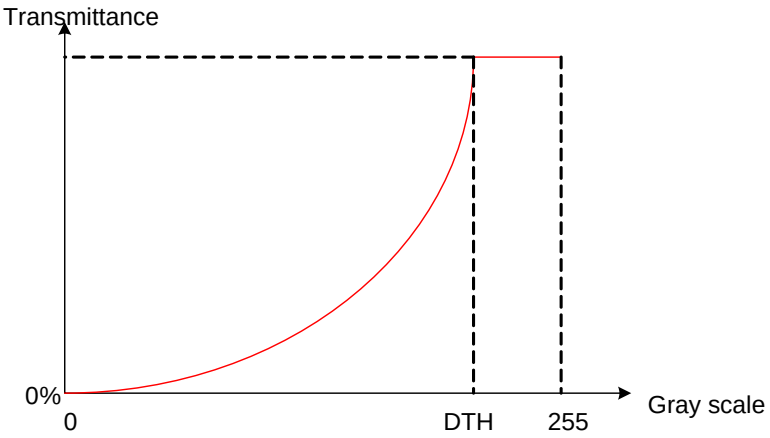
Description

DTH_MOV [3:0]: This parameter is used to set the minimum limitation of grayscale threshold value in Moving Image mode.

DTH_MOV[3:0]				Description	DTH_MOV[3:0]				Description
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	224	1	0	0	0	192
0	0	0	1	220	1	0	0	1	188
0	0	1	0	216	1	0	1	0	184
0	0	1	1	212	1	0	1	1	180
0	1	0	0	208	1	1	0	0	176
0	1	0	1	204	1	1	0	1	172
0	1	1	0	200	1	1	1	0	168
0	1	1	1	196	1	1	1	1	164

DTH_STILL [3:0]: This parameter is used to set the minimum limitation of grayscale threshold value in Still Picture mode.

DTH_STILL[3:0]				Description	DTH_STILL[3:0]				Description
D3	D2	D1	D0		D3	D2	D1	D0	
0	0	0	0	224	1	0	0	0	192
0	0	0	1	220	1	0	0	1	188
0	0	1	0	216	1	0	1	0	184
0	0	1	1	212	1	0	1	1	180
0	1	0	0	208	1	1	0	0	176
0	1	0	1	204	1	1	0	1	172
0	1	1	0	200	1	1	1	0	168
0	1	1	1	196	1	1	1	1	164



Restriction: To enable this command, “Page 5 Command Set enable register (FFh) ” must set first.

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<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DTH_MOV[3:0]</th><th>DTH_STILL[3:0]</th></tr>
<tr><td>Power ON Sequence</td><td>4’hA</td><td>4’h8</td></tr>
<tr><td>S/W Reset</td><td>No change</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>4’hA</td><td>4’h8</td></tr>
</table>
</td></tr>
</table>

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4.8.5. Backlight Control 5 (04h)

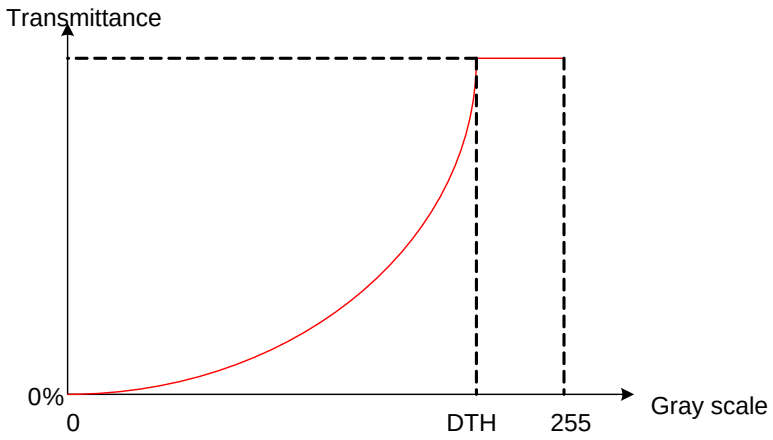
Page 5 Command Set		04h : BLCTRL5 (Backlight Control 5)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	0	04h
1st Parameter	Write / Read	0	0	0	0	DTH_UI[3:0]				04h

Description

DTH_UI [3:0]: This parameter is used to set the minimum limitation of grayscale threshold value in UI (User Interface Image mode).

DTH_UI[3:0]				Description
D3	D	D1	D0	
0	0	0	0	252
0	0	0	1	248
0	0	1	0	244
0	0	1	1	240
0	1	0	0	236
0	1	0	1	232
0	1	1	0	228
0	1	1	1	224

DTH_UI[3:0]				Description
D3	D2	D1	D0	
1	0	0	0	220
1	0	0	1	216
1	0	1	0	212
1	0	1	1	208
1	1	0	0	204
1	1	0	1	200
1	1	1	0	196
1	1	1	1	192



Restriction: To enable this command, “Page 5 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DTH_UI
Power ON Sequence	4’h4
S/W Reset	No change
H/W Reset	4’h4

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4.8.6. Backlight Control 6 (05h)

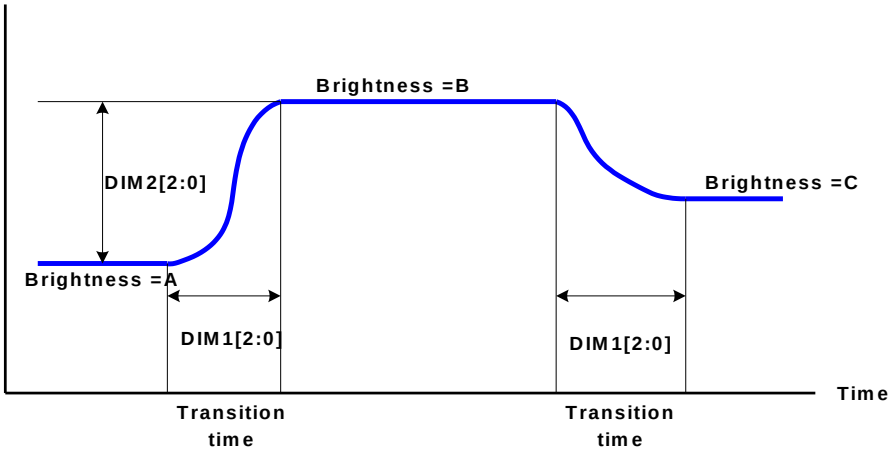
Page 5 Command Set		05h : BLCTRL6 (Backlight Control 6)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	0	1	05h
1st Parameter	Write / Read	0	DIM_MOV[2:0]			0	DIM_STILL[2:0]			43h

Description

DIM_STILL[2:0]: This parameter is used to set the transition time of brightness level change to avoid the sharp brightness change on vision in Still Picture mode.

DIM_MOV[2:0]: This parameter is used to set the transition time of brightness level change to avoid the sharp brightness change on vision in Moving Image mode.

DIM_MOV[2 :0]/ DIM_STILL[2 :0]			Description
D2	D1	D0	
0	0	0	2 frame
0	0	1	3 frame
0	1	0	4 frames
0	1	1	6 frames
1	0	0	10 frames
1	0	1	18 frames
1	1	0	34 frames
1	1	1	66 frames



*Note: **DIM1[2:0]** mean **DIM_MOV[2:0]** or **DIM_STILL[2:0]** or **DIM_UI[2:0]** in different mode.*

Restriction: To enable this command, "Page 5 Command Set enable register (FFh) " must set first.

Register Availability

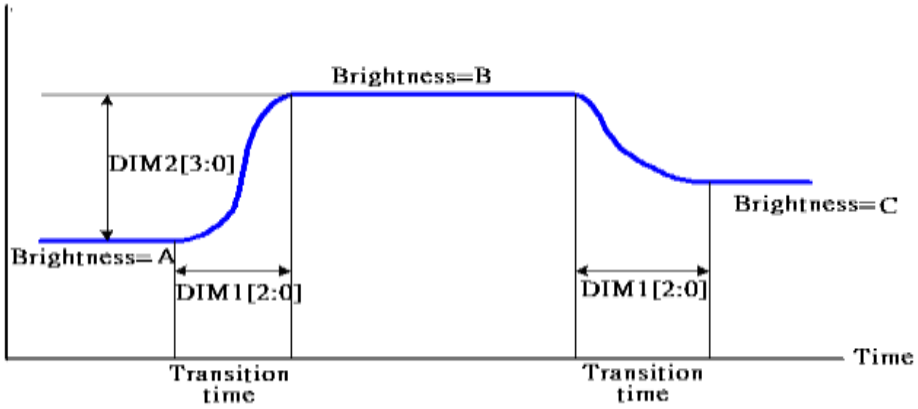
Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIM_MOV[2:0]	DIM_STILL[2:0]
Power ON Sequence	3'h4	3'h3
S/W Reset	No change	No change
H/W Reset	3'h4	3'h3

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4.8.7. Backlight Control 7 (06h)

<table>
<tr><th colspan="2">Page 5 Command Set</th><th colspan="9">06h : BLCTRL7 (Backlight Control 7)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>06h</td></tr>
<tr><td>1st Parameter</td><td>Write / Read</td><td colspan="4">DIM_MIN[3:0]</td><td>0</td><td colspan="3">DIM_UI[2:0]</td><td>02h</td></tr>
<tr><td>Description</td><td colspan="10">
DIM_UI[2:0]: This parameter is used to set the transition time of brightness level change to avoid the sharp brightness change on vision in UI mode (User Interface Image mode).
<table>
<tr><th colspan="3">DIM_UI[2:0]</th><th rowspan="2">Description</th></tr>
<tr><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>2 frame</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>3 frame</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>4 frames</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>6 frames</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>10 frames</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>18 frames</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>34 frames</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>66 frames</td></tr>
</table>


Note1: DIM1[2:0] means DIM_MOV[2:0] or DIM_STILL[2:0] or DIM_UI[2:0] in different mode.
Note2: DIM2[3:0] means DIM_MIN[3:0].
DIM_MIN [3:0]: This parameter is used to set the imitation of minimum brightness change. If this parameter is large than the difference between target brightness and current brightness, then the brightness will not change.
</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 5 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DIM_MIN[3:0]</th><th>DIM_UI[2:0]</th></tr>
<tr><td>Power ON Sequence</td><td>4’h0</td><td>3’h2</td></tr>
<tr><td>S/W Reset</td><td>No change</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>4’h0</td><td>3’h2</td></tr>
</table>
</td></tr>
</table>

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4.8.8. Backlight Control 8 (07h)

Page 5 Command Set		07h : BLCTRL8 (Backlight Control 8)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	1	1	07h
1st Parameter	Write / Read	LABS_SRE_THR[3:0]				LABC SRE ENABLE	LEDONR	LEDONPOL	PWMPOL	B0h

Description

PWMPOL: The bit is used to define polarity of LEDPWM signal.

BL	PWMPOL	LEDPWM pin
0	0	Always low
0	1	Always high
1	0	Original polarity of PWM signal
1	1	Inversed polarity of PWM signal

LEDONPOL: This bit is used to control LEDON pin.

BL	LEDONPOL	LEDON pin
0	0	0
0	1	1
1	0	LEDONR
1	1	Inversed LEDONR

LEDONR: This bit is used to control LEDON pin.

LEDONR	Description
0	Low
1	High

LABCSREENABLE: The bit enables SRE function.

LABS_SRE_THR[3:0]:

The threshold value of LABC to turn-on SRE with hysteresis if LABC_SRE_ENABLE=1

AmbientLightSensor[7:0]>=LABC_SRE_THE[3:0]*16, turn-on SRE

AmbientLightSensor[7:0]<=(LABC_SRE_THE[3:0]-1)*16, turn-off SRE

Restriction

1. To enable this command, “Page 5 Command Set enable register (FFh) ” must set first.
2. The setting of LABC_SRE_THE[3:0] must be over 1 hex or equal 1 hex.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	LABS_SRE_THR[3:0]	LABCSRE ENABLE	LEDONR	LEDONPOL	PWMPOL
Power On Sequence	4’hB	1’h0	1’h0	1’h0	1’h0
S/W Reset	No change	No change	No change	No change	No change
H/W Reset	4’hB	1’h0	1’h0	1’h0	1’h0

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4.8.9. Backlight Control 9 (09h)

Page 5 Command Set		09h : BLCTRL9 (Backlight Control 9)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	0	0	1	09h
1st Parameter	Write / Read	SRECABC BOOSTEN	1	1	1	SRECABC EN	1	0	0	74h
Description	**SRECABCBOOSTEN**: The bit boosts the SRE function. **SRECABCEN:** The bit enables SRE function.									
Restriction	To enable this command, "Page 5 Command Set enable register (FFh) " must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	SRECABC BOOSTEN	SRECABC EN
Power On Sequence	1'h0	1'h0
S/W Reset	No change	No change
H/W Reset	1'h0	1'h0

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4.8.10. Backlight Control 10 (0Ch)

Page 5 Command Set		0Ch : BLCTRL10 (Backlight Control 10)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	1	1	0	0	0Ch
1st Parameter	Write / Read	ALS8BIT[7:0]								A0h
Description	**ALS8BIT[7:0]**: This command is used to give an ambient light information.									
Restriction	To enable this command, “Page 5 Command Set enable register (FFh) ” must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	ALS8BIT[7:0]
Power ON Sequence	8’hA0
S/W Reset	No change
H/W Reset	8’hA0

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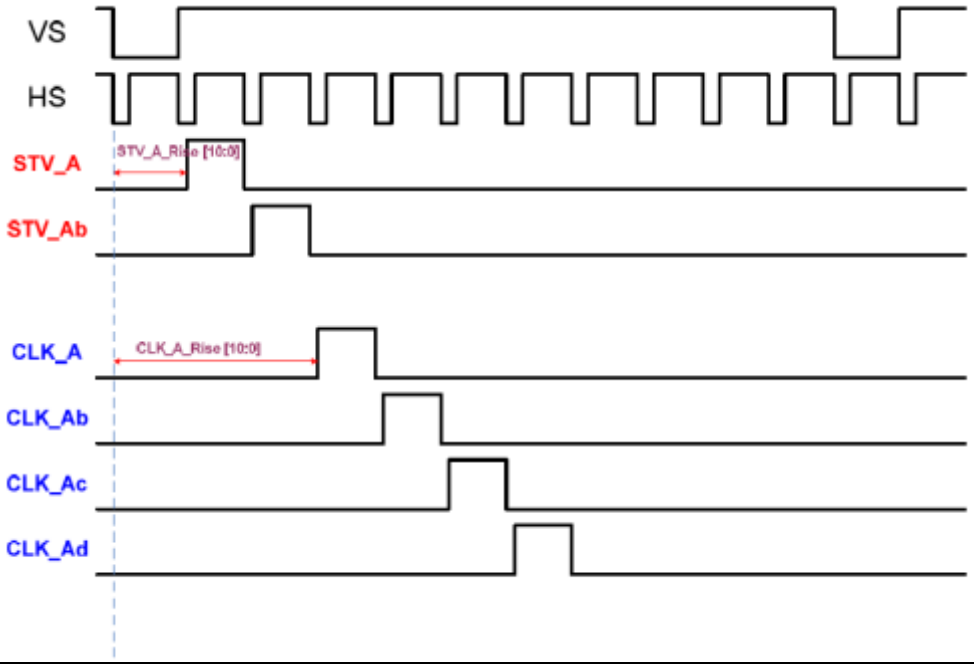
4.9. Page 6 Command Description

4.9.1. GIP Setting (00h~1Dh / 20h~27h / 30h~40h)

Page 6 Command Set										
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
00h	Write / Read	**F_TIME_OPT**	**STV_A_Rise[9:8]**		GIP_0_SET0					
01h	Write / Read	**STV_A_Rise[7:0]**								-
02h	Write / Read	GIP_0_SET1								-
03h	Write / Read	GIP_0_SET2								-
04h	Write / Read	GIP_0_SET3								-
05h	Write / Read	GIP_0_SET4								-
06h	Write / Read	**CLK_A_Rise[10:8]**			GIP_0_SET5					-
07h	Write / Read	**CLK_A_Rise[7:0]**								-
08h	Write / Read	GIP_0_SET6								-
09h	Write / Read	GIP_0_SET7								-
0Ah	Write / Read	GIP_0_SET8								-
0Bh	Write / Read	GIP_0_SET9								-
0Ch	Write / Read	GIP_0_SET10								-
0Dh	Write / Read	GIP_0_SET11								-
0Eh	Write / Read	GIP_0_SET12								-
0Fh	Write / Read	GIP_0_SET13								-
10h	Write / Read	GIP_0_SET14								-
11h	Write / Read	GIP_0_SET15								-
12h	Write / Read	GIP_0_SET16								-
13h	Write / Read	GIP_0_SET17								-
14h	Write / Read	GIP_0_SET18								-
15h	Write / Read	GIP_0_SET19								-
16h	Write / Read	GIP_0_SET20								-
17h	Write / Read	GIP_0_SET21								-
18h	Write / Read	GIP_0_SET22								-
19h	Write / Read	GIP_0_SET23								-
1Ah	Write / Read	GIP_0_SET24								-
1Bh	Write / Read	GIP_0_SET25								-
1Ch	Write / Read	GIP_0_SET26								-
1Dh	Write / Read	GIP_0_SET27								-

Page 6 Command Set										
Command	Write / Read	Parameter								Default (Hex)
		D7	D6	D5	D4	D3	D2	D1	D0	
20h	Write / Read	GIP_1_SET0								-
21h	Write / Read	GIP_1_SET1								-
22h	Write / Read	GIP_1_SET2								-
23h	Write / Read	GIP_1_SET3								-
24h	Write / Read	GIP_1_SET4								-
25h	Write / Read	GIP_1_SET5								-
26h	Write / Read	GIP_1_SET6								-
27h	Write / Read	GIP_1_SET7								-

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<table>
<tr><th colspan="11">Page 6 Command Set</th></tr>
<tr><th rowspan="2">Command</th><th rowspan="2">Write / Read</th><th colspan="8">Parameter</th><th rowspan="2">Default (Hex)</th></tr>
<tr><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>30h</td><td>Write / Read</td><td colspan="8">GIP_2_SET0</td><td>-</td></tr>
<tr><td>31h</td><td>Write / Read</td><td colspan="8">GIP_2_SET1</td><td>-</td></tr>
<tr><td>32h</td><td>Write / Read</td><td colspan="8">GIP_2_SET2</td><td>-</td></tr>
<tr><td>33h</td><td>Write / Read</td><td colspan="8">GIP_2_SET3</td><td>-</td></tr>
<tr><td>34h</td><td>Write / Read</td><td colspan="8">GIP_2_SET4</td><td>-</td></tr>
<tr><td>35h</td><td>Write / Read</td><td colspan="8">GIP_2_SET5</td><td>-</td></tr>
<tr><td>36h</td><td>Write / Read</td><td colspan="8">GIP_2_SET6</td><td>-</td></tr>
<tr><td>37h</td><td>Write / Read</td><td colspan="8">GIP_2_SET7</td><td>-</td></tr>
<tr><td>38h</td><td>Write / Read</td><td colspan="8">GIP_2_SET8</td><td>-</td></tr>
<tr><td>39h</td><td>Write / Read</td><td colspan="8">GIP_2_SET9</td><td>-</td></tr>
<tr><td>3Ah</td><td>Write / Read</td><td colspan="8">GIP_2_SET10</td><td>-</td></tr>
<tr><td>3Bh</td><td>Write / Read</td><td colspan="8">GIP_2_SET11</td><td>-</td></tr>
<tr><td>3Ch</td><td>Write / Read</td><td colspan="8">GIP_2_SET12</td><td>-</td></tr>
<tr><td>3Dh</td><td>Write / Read</td><td colspan="8">GIP_2_SET13</td><td>-</td></tr>
<tr><td>3Eh</td><td>Write / Read</td><td colspan="8">GIP_2_SET14</td><td>-</td></tr>
<tr><td>3Fh</td><td>Write / Read</td><td colspan="8">GIP_2_SET15</td><td>-</td></tr>
<tr><td>40h</td><td>Write / Read</td><td colspan="8">GIP_2_SET16</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">F_TIME_OPT: The command set the GIP timing Mode.
<table>
<tr><th>F_TIME_OPT</th><th>Description</th></tr>
<tr><td>0</td><td>refer to internal OSC counter</td></tr>
<tr><td>1</td><td>refer to Hsync</td></tr>
</table>

</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 6 Command Set enable register (FFh) ” must set first.</td></tr>
</table>

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Register Availability	

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

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4.9.2. GOUT_VGLO Control 1 (52h)

Page 6 Command Set		52h : GVLOCTRL 1(GOUT_VGLO Control 1)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	0	52h
1st Parameter	Write / Read	0	0	0	1	GOUT_VGLO_SO[3:0]				11h

Description

GOUT_VGLO_SO [3:0]: The command sets the GIP power source of GOUT_VGLO at Sleep-Out Mode.

GOUT_VGLO_SO [3:0]				Description
0	0	0	0	VGL
0	0	0	1	GND
0	0	1	0	VGL_REG
0	0	1	1	Inhibited
0	1	0	0	Inhibited
0	1	0	1	Inhibited
0	1	1	0	Inhibited
0	1	1	1	Inhibited

Restriction

To enable this command, “Page 6 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GOUT_VGLO_SO [3:0]
Power ON Sequence	4’h0
S/W Reset	No change
H/W Reset	4’h0

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4.9.3. GOUT_VGLO Control 2(53h)

Page 6 Command Set		53h : GVLOCTRL 2(GOUT_VGLO Control 2)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	0	1	1	53h
1st Parameter	Write / Read	0	0	0	1	GOUT_VGLO_DSP[3:0]				10h

Description

GOUT_VGLO_DSP [3:0]: The command sets the GIP power source of GOUT_VGLO at Display On Mode.

GOUT_VGLO_DSP [3:0]				Description
0	0	0	0	VGL
0	0	0	1	GND
0	0	1	0	VGL_REG
0	0	1	1	Inhibited
0	1	0	0	Inhibited
0	1	0	1	Inhibited
0	1	1	0	Inhibited
0	1	1	1	Inhibited

Restriction

To enable this command, “Page 6 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GOUT_VGLO_DSP [3:0]
Power ON Sequence	4’h0
S/W Reset	No change
H/W Reset	4’h0

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4.9.4. GOUT_VGHO Control (54h)

Page 6 Command Set		54h : GVHOCTRL (GOUT_VGHO Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	1	0	1	0	1	0	0	54h
1st Parameter	Write / Read	0	GOUT_VGHO[2:0]			GOUT_VGLO_LVD[3:0]				11h

Description

GOUT_VGHO [2:0]: The command sets the GIP power source of GOUT_VGHO.

GOUT_VGHO [2:0]			Description
0	0	0	VGH_REG
0	0	1	VGH
0	1	0	Inhibited
0	1	1	Inhibited
1	0	0	Inhibited
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

GOUT_VGLO_LVD [3:0]: The command sets the GIP power source of GOUT_VGLO at LVD detect.

GOUT_VGLO_LVD [3:0]				Description
0	0	0	0	VGL
0	0	0	1	GND
0	0	1	0	VGL_REG
0	0	1	1	VGH
0	1	0	0	Inhibited
0	1	0	1	Inhibited
0	1	1	0	Inhibited
0	1	1	1	Inhibited

Restriction

To enable this command, “Page 6 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	GOUT_VGHO [2:0]	GOUT_VGLO_LVD [3:0]
Power ON Sequence	3’h1	4’h1
S/W Reset	No change	No change
H/W Reset	3’h1	4’h1

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4.10. Page 7 Command Description

4.10.1. CLAMP Control (00h)

Page 7 Command Set		00h : CLPCTRL (Clamp Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	0	0	00h
1st Parameter	Write / Read	0	1	0	1	0	VDH_CLP_EN	0	1	55h

Description

VDH_CLP_EN : The bit is enable the clamp function of DDVDH.

VDH_CLP_EN	Description
0	Disable
1	Enable

Restriction

To enable this command, “Page 7 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VDH_CLP_EN
Power ON Sequence	1’h1
S/W Reset	No change
H/W Reset	1’h1

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4.10.2. Power Bias Control (02h)

Page 7 Command Set		02h : PWBCTRL (Power Bias Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	0	1	0	02h
1st Parameter	Write / Read	0	DDVDL_CLP_ISC [2:0]			0	DDVDH_CLP_ISC [2:0]			00h

Description

DDVDL_CLP_ISC [2:0] : DDVDL Clamp OP bias control.

DDVDL_CLP _ISC [2:0]			DDVDL clamp bias (uA)
0	0	0	2
0	0	1	4
0	1	0	6
0	1	1	8
1	0	0	10
1	0	1	12
1	1	0	14
1	1	1	16

DDVDH_CLP _ISC [2:0] : DDVDH Clamp OP bias control.

DDVDH_CLP_ISC [2:0]			DDVDH clamp bias (uA)
0	0	0	2
0	0	1	4
0	1	0	6
0	1	1	8
1	0	0	10
1	0	1	12
1	1	0	14
1	1	1	16

Restriction: To enable this command, “Page 7 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DDVDL_CLP _ISC [2:0]	DDVDH_CLP _ISC [2:0]
Power ON Sequence	3’h0	3’h0
S/W Reset	No change	No change
H/W Reset	3’h0	3’h0

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4.10.3. VCL Control (06h)

Page 7 Command Set		06h : VCLCTRL (VCL Control)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	0	0	1	1	0	06h
1st Parameter	Write / Read	0	0	0	VCLOPT	0	0	VCL_CLP[1:0]		01h

Description

VCLOPT : VCL voltage control.

VCLOPT	VCL Voltage
0	VCI X -1
1	VCI X -2

VCL_CLP[1:0] : Sets the VCL clamp level.

VCL_CLP[1:0]		VCL clamp level (V)
0	0	-2.8
0	1	-3.0
1	0	-3.2
1	1	-3.4

Restriction: To enable this command, “Page 7 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	VCLOPT	VCL_CLP[1:0]
Power ON Sequence	1’h0	2’h1
S/W Reset	No change	No change
H/W Reset	1’h0	2’h1

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4.10.4. VGL_REG ENABLE (17h)

Page 7 Command Set		17h : VGLREGEN (VGL_REG EN)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	0	0	0	1	0	1	1	1	17h
1st Parameter	Write / Read	0	0	1	VGLREG_EN	0	0	1	0	22h

Description

VGLREG_EN : The bit is enable the VGL_REG.

VGLREG_EN	Description
0	Disable
1	Enable

Note : The voltage setting of VGL_REG in Section 4.4.21

Restriction

To enable this command, “Page 7 Command Set enable register (FFh) ” must set first.

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GOUT_VGHO [2:0]
Power ON Sequence	3’h1
S/W Reset	No change
H/W Reset	3’h1

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4.10.5. VREG1/2OUT ENABLE (18h)

<table>
<tr><th colspan="2">Page 7 Command Set</th><th colspan="8">18h : VREG12EN (VREG1/2OUT ENABLE)</th></tr>
<tr><td></td><td>Write / Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default (Hex)</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>18h</td></tr>
<tr><td>1st Parameter</td><td>Write / Read</td><td>0</td><td>0</td><td>0</td><td>VREG EN</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>Description</td><td colspan="10">VREGEN : The bit enables VREG1OUT and VREG2OUT .
<table><tr><th>VREGEN</th><th>Description</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>
Note : The voltage setting of VREG1OUT and VREG2OUT is in Sections 4.4.24 and 4.4.25</td></tr>
<tr><td>Restriction</td><td colspan="10">To enable this command, “Page 7 Command Set enable register (FFh) ” must set first.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VREG EN</th></tr><tr><td>Power ON Sequence</td><td>1’h0</td></tr><tr><td>S/W Reset</td><td>No change</td></tr><tr><td>H/W Reset</td><td>1’h0</td></tr></table></td></tr>
</table>

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4.10.6. LVD OPTION (B3h)

Page 7 Command Set		B3h : LVDOP (LVD Option)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	0	1	1	0	0	1	1	B3h
1st Parameter	Write / Read	0	0	LVD_OP [1:0]		0	0	0	0	00h
Description	**LVD_OP[1:0]** : The command sets the GOUT level at LVD detect.									
Restriction	To enable this command, "Page 7 Command Set enable register (FFh) " must set first.									
Register Availability										
Default										

LVD_OP [1:0]		GOUT Level
0	0	GND
0	1	VGH
1	0	Inhibited
1	1	Inhibited

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
	LVD_OP [1:0]
Power ON Sequence	2'h0
S/W Reset	No change
H/W Reset	2'h0

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4.10.7. TIME CONTROL (E1h)

Page 7 Command Set		E1h : TIMECTRL (TIME CONTROL)								
	Write / Read	D7	D6	D5	D4	D3	D2	D1	D0	Default (Hex)
Command	Write	1	1	1	0	0	0	0	1	E1h
1st Parameter	Write / Read	TIME_SHIFT_ERR[3:0]				1	0	0	1	09h
Description	**TIME_SHIFT_ERR[3:0]** : Timming Option.									
Restriction	To enable this command, “Page 7 Command Set enable register (FFh) ” must set first.									

Register Availability

Status	Availability
Normal Mode On, Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	TIME_SHIFT_ERR [3:0]
Power ON Sequence	4’h0
S/W Reset	No change
H/W Reset	4’h0

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5. Sleep Out Command and Self-Diagnostic Functions

5.1. Register loading Detection

Sleep Out command (See “Sleep Out (11h of the Page 0)”) is a trigger for an internal function of the display module, which indicates that if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller does work properly.

There are compared factory values of the OTP and register values of the display controller by the display controller (1st step: Compares register and OTP values, 2nd step: Loads OTP value to register). If both values (OTP and register values) are the same, there is inverted (= increased by 1) bit, which is defined in command Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If these values are not same, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

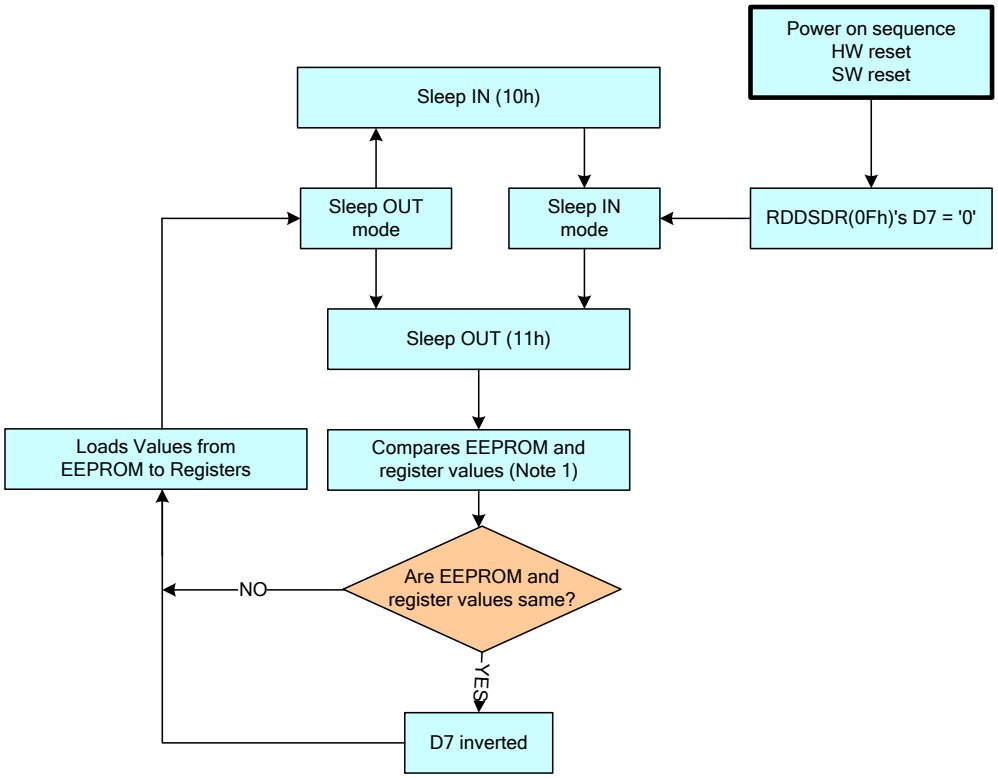


Figure 94 Register loading Detection

Note :

1. If the OTP and register values are not compared and loaded, they can be changed by commands 00h to AFh and DAh to DDh..
2. This information is only used if TE line is used.

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5.2. Functionality Detection

The Sleep Out command (See “Sleep Out (11h of the Page 0)”) is a trigger for an internal function of the display module. It indicates if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (= increased by 1), which defined in the command “Read Display Self-Diagnostic Result (0Fh)” (RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (not increased by 1).The flow chart for this internal function is following:

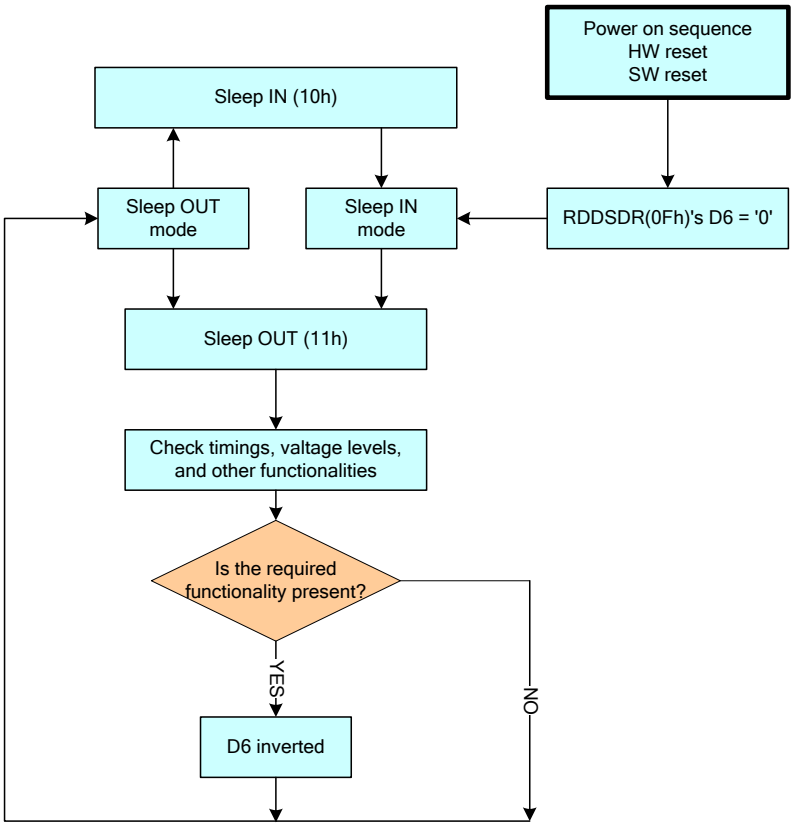


Figure 95 Functionality Detection

Note:

1. When changing from the Sleep In mode to the Sleep Out mode, 120msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and the value of RDDSDR’s D6 is valid. Otherwise, there will be 5msec delay for the D6’s value to be valid when the Sleep Out command is sent in the Sleep Out mode.
2. This function is only used if TE-line is used.

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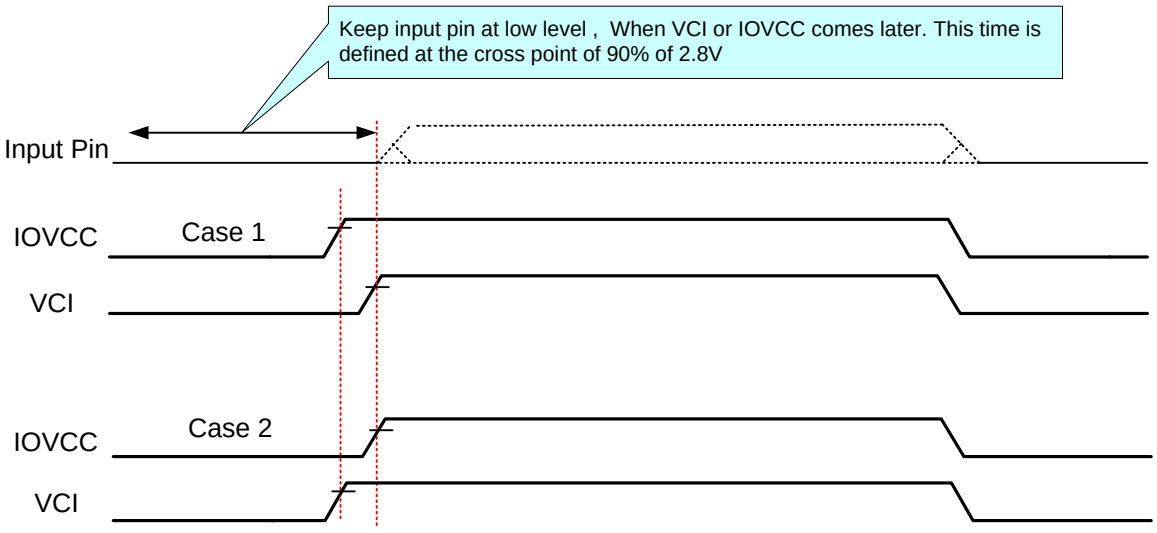
6. Power ON/OFF Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note:

1. There will be no damage to ILI9806E-2C if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 6.1 and 6.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep input pins at low level, when VCI or IOVCC comes later.

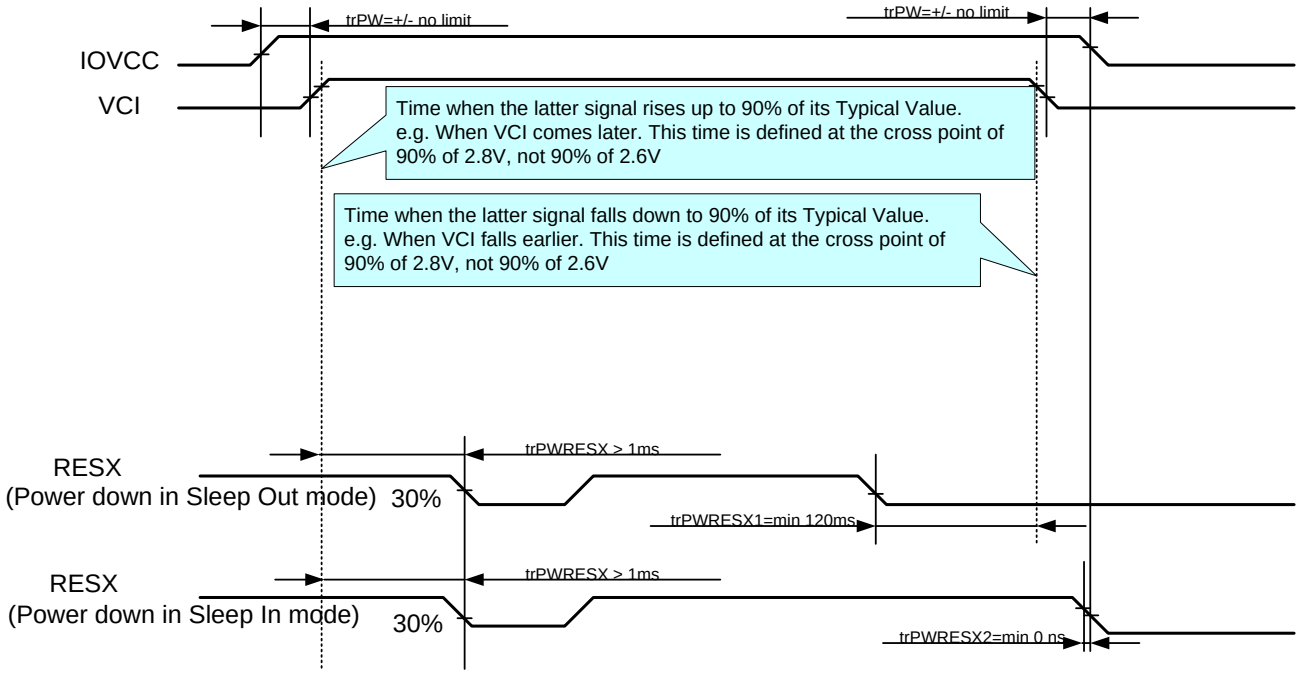
Input Pin Name							
IM[3:0]	RESX	CSX	SCL	DB[23:0]	SDI (SDA)	PCLK	VS
HS	DE	HS_CP	HS_CN	HS_D0P	HS_D0N	HS_D1P	HS_D1N



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6.1. Case 1 –RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

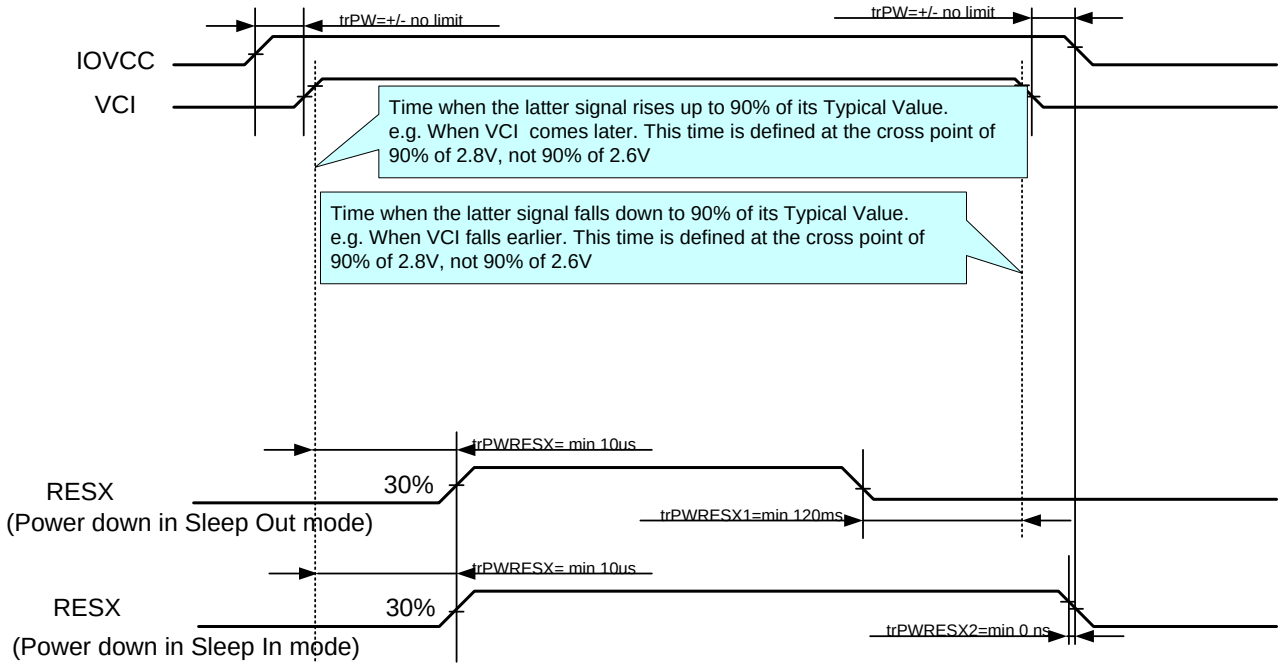
Notes :
1. The VCI / IOVCC slew rate ≥ 100us

Figure 96 Case 1 – RESX line is held High or Unstable by Host at Power ON

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6.2. Case 2 – RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note : The VCI / IOVCC slew rate ≥ 100us

Figure 97 Case 2 – RESX line is held Low by Host at Power ON

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6.3. Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, ILI9806E-2C will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up.

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7. Power Level Definition

7.1. LCM Voltage Generation

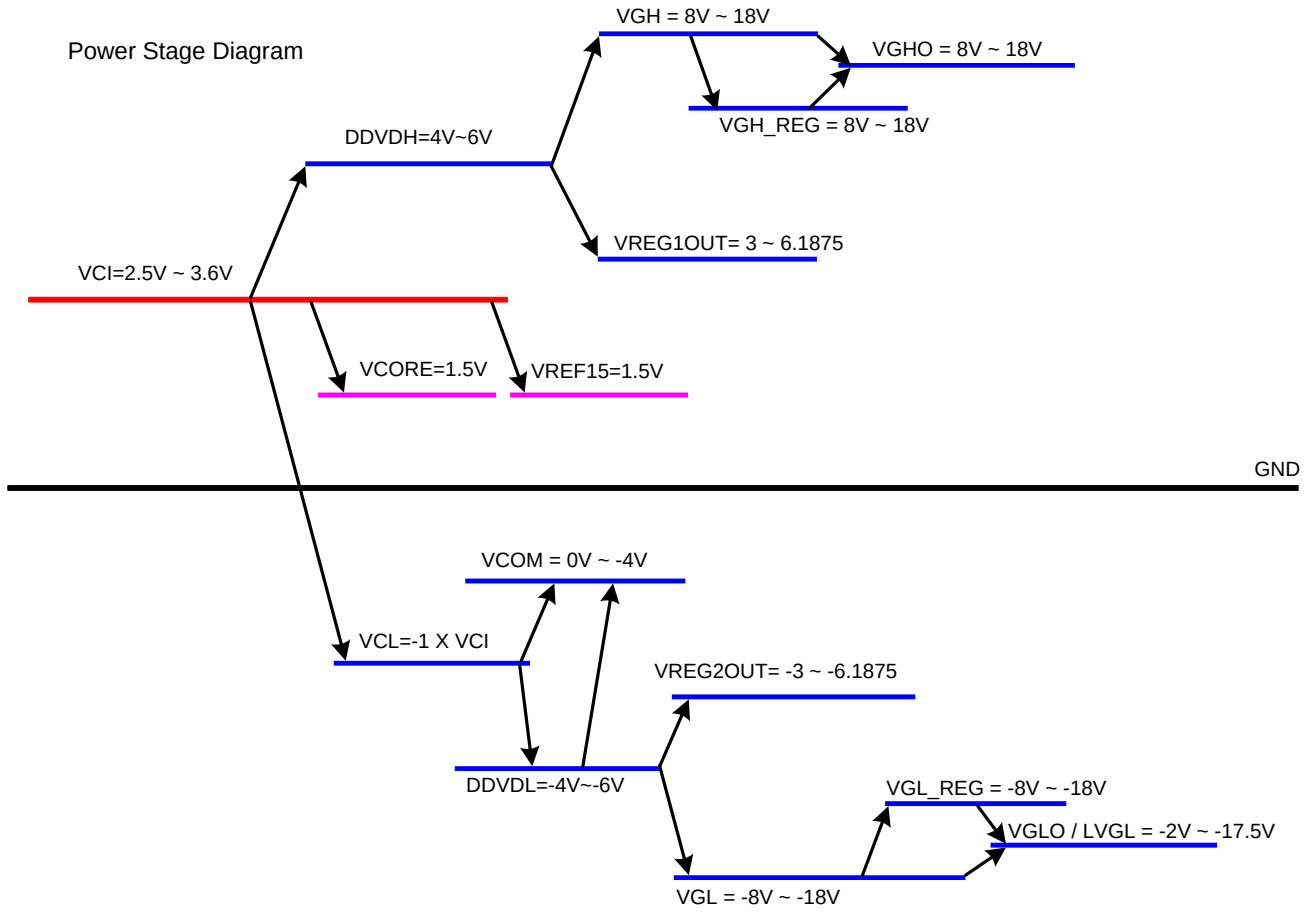


Figure 98 Power Stage Diagram

Note: 1. The DDVDH, DDVDL, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to current consumption at respective outputs.

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7.2. Gamma Curves

7.2.1. Gamma Curve 1 (GC0) , applies the function y=x^2.2

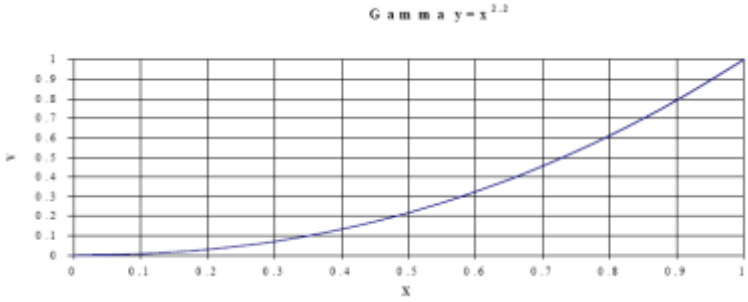


Figure 99 Gamma Curve 1 (GC0)

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8. Reset

8.1. Driver IC Input and Output pins

8.1.1. Output Pins, I/O Pins

Table 39 Output and I/O Pins

Pin/Line	After Power ON	After Hardware Reset	After Software Reset
DB [23:0]	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
SDA (Output direction), SDO	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HS_D0P	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HS_D0N	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
TE_L, TE_R	Low	Low	Low
LEDPWM	Low	Low	Low

Note: 1. There will be no output from DB [23:0], SDA, SDO, LEDPWM, TE, HS_D0P, HS_D0N, during Power ON/OFF sequence, hardware reset and software reset.

8.1.2. Input Pins

Table 40 Input Pins

Pin/Line	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 7	Input valid	Input valid	Input valid	See Chapter 6
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
DCX	Input invalid	Input valid	Input valid	Input valid	Input invalid
SCL	Input invalid	Input valid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS	Input invalid	Input valid	Input valid	Input valid	Input invalid
VS	Input invalid	Input valid	Input valid	Input valid	Input invalid
PCLK	Input invalid	Input valid	Input valid	Input valid	Input invalid
DB [23:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
SDA (input direction), SDI	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_CP	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_CN	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_D0P	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_D0N	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_D1P	Input invalid	Input valid	Input valid	Input valid	Input invalid
HS_D1N	Input invalid	Input valid	Input valid	Input valid	Input invalid

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8.1.3. Reset Timing

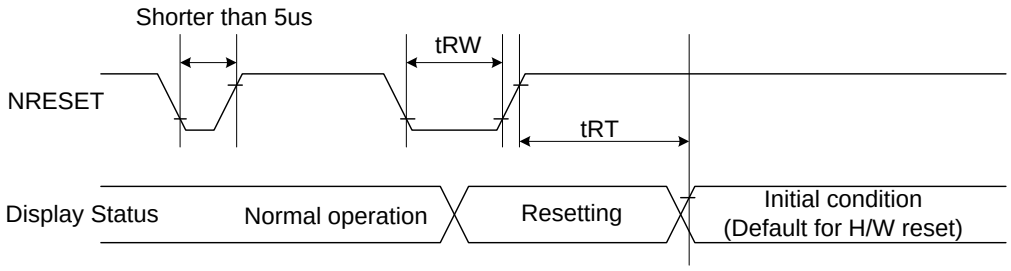


Figure 100 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 42.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

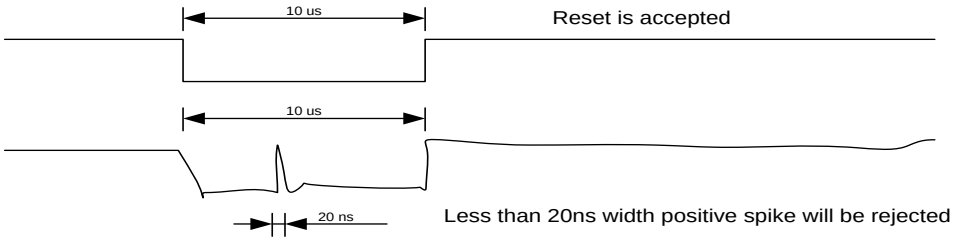


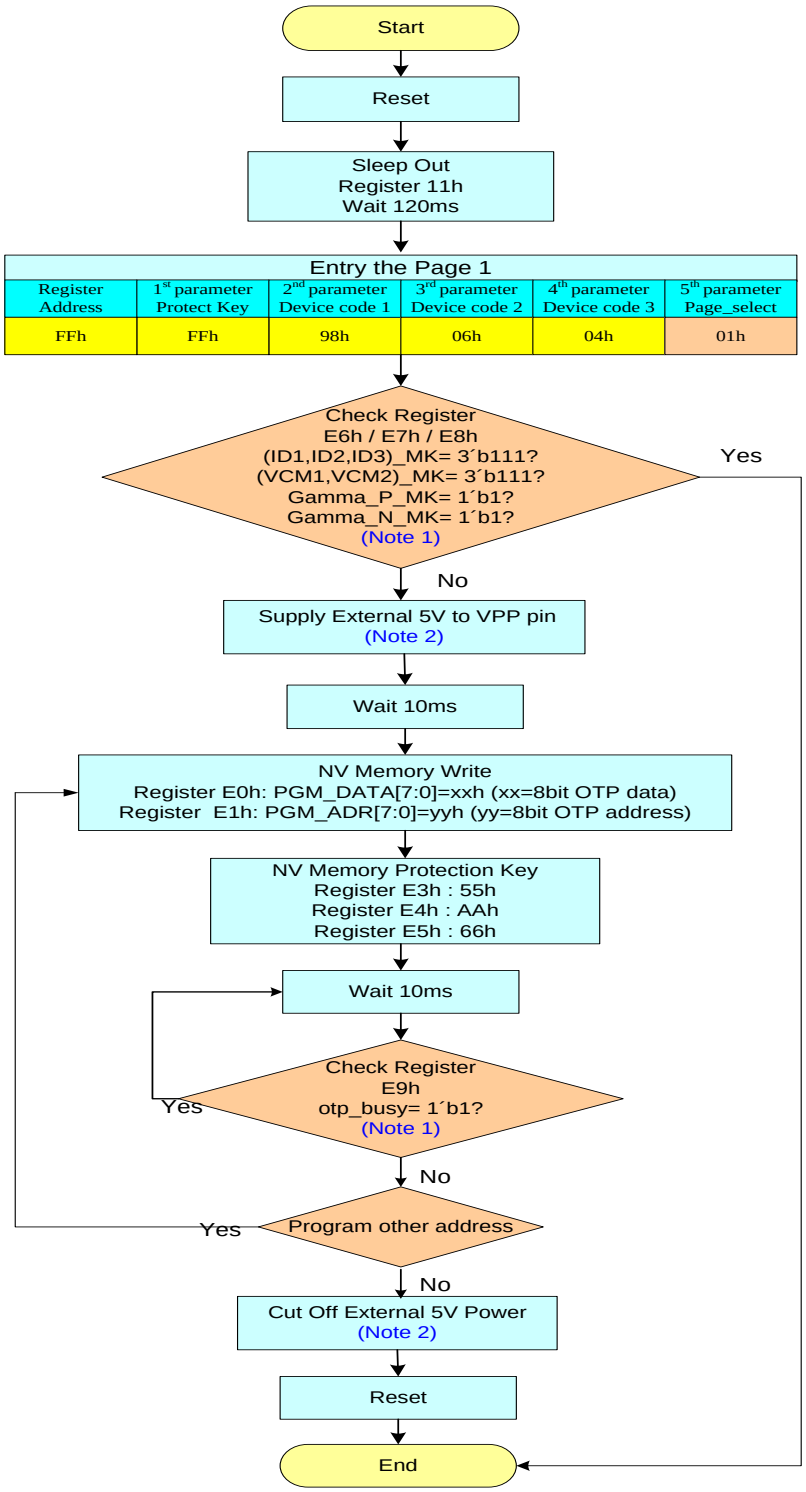
Figure 101 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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9. NV Memory Programming

9.1. NV Memory Programming flow



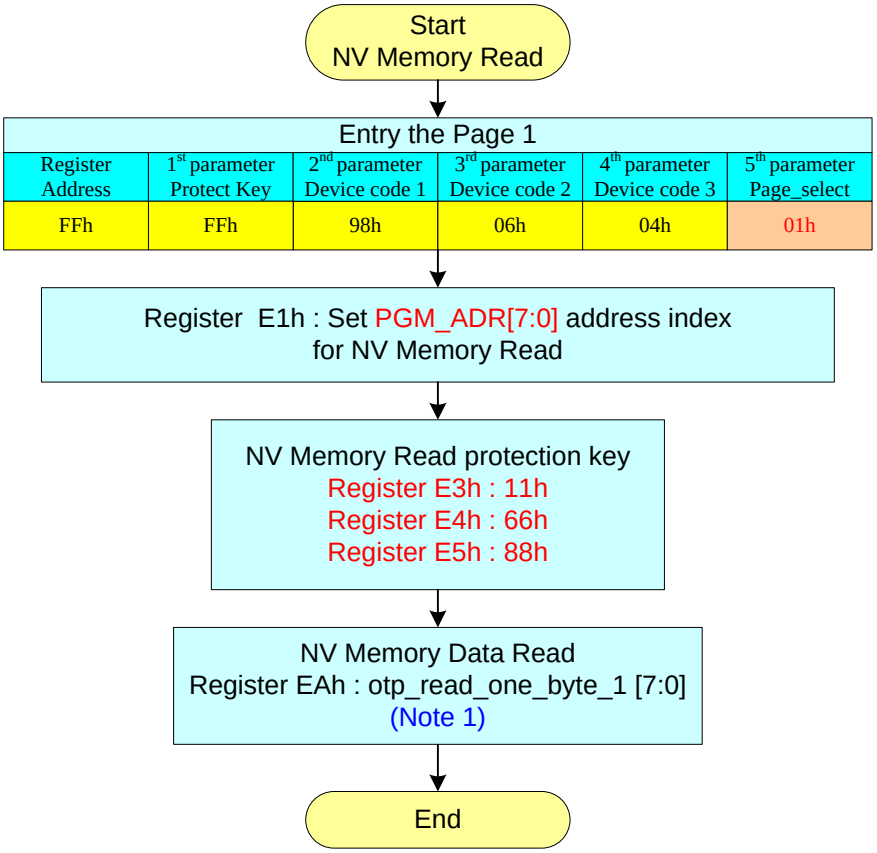
Note 1: In SPI operation mode, set register FEh "ext_spi_read_en"=1 to enable the read function of extend command and "ext_spi_read_en"=0 to return to the write mode

Note 2 :If user want to use the internal programming , do not execute this step also can finish the programming flow

Figure 102 NV Memory Programming Flow

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9.2. NV Memory Read flow



Note 1: In SPI operation mode, set register FEh "ext_spi_read_en"=1 to enable the read function of extend command and "ext_spi_read_en"=0 to return to the write mode

Figure 103 NV Memory Read Flow

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10. Gamma Correction

Positive Gamma Control (Page1_A0h~AFh)

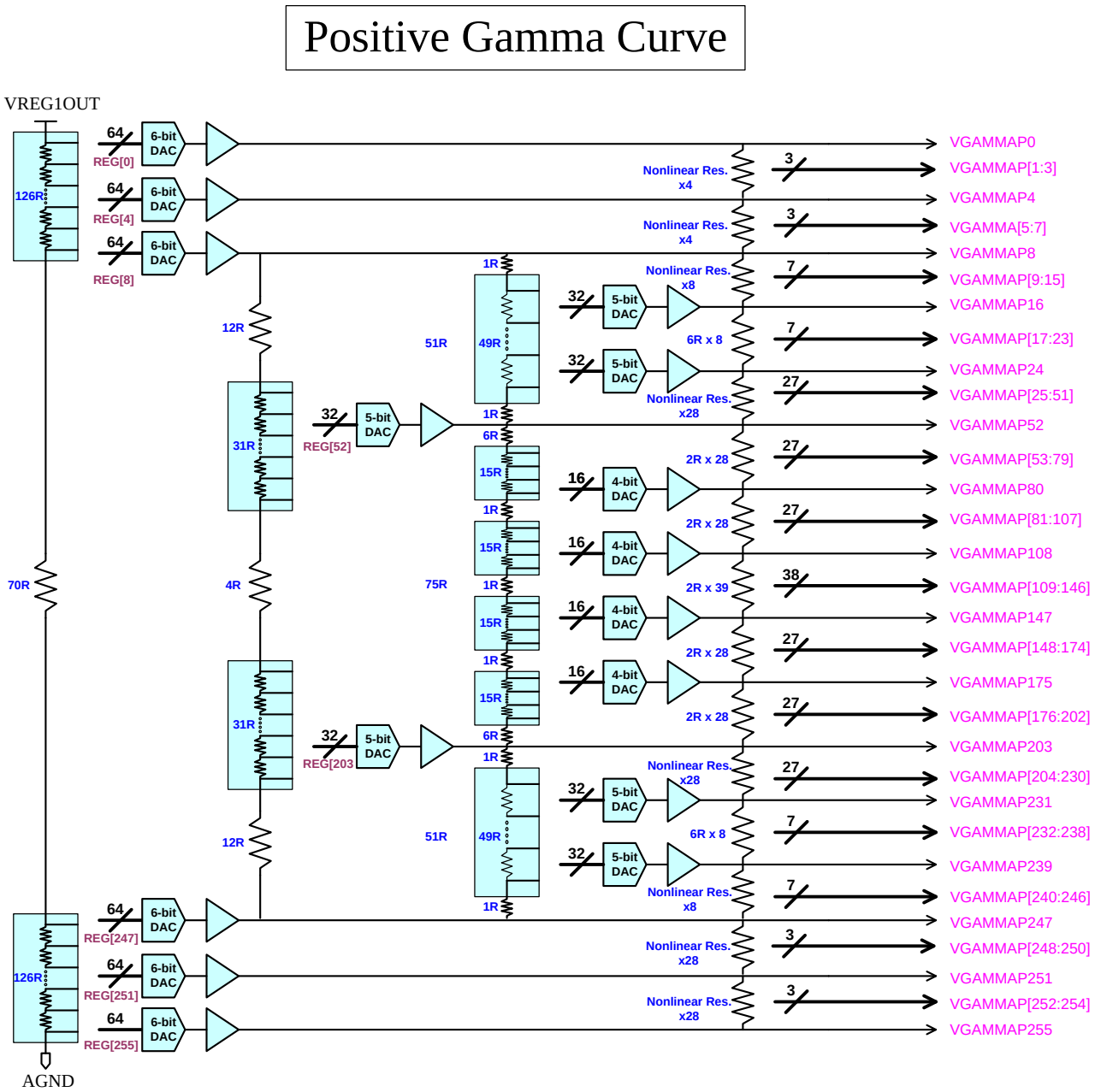


Figure 104 Positive Gamma Control (Page1_A0h~AFh)

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Negative Gamma Control (Page1_C0h~CFh)

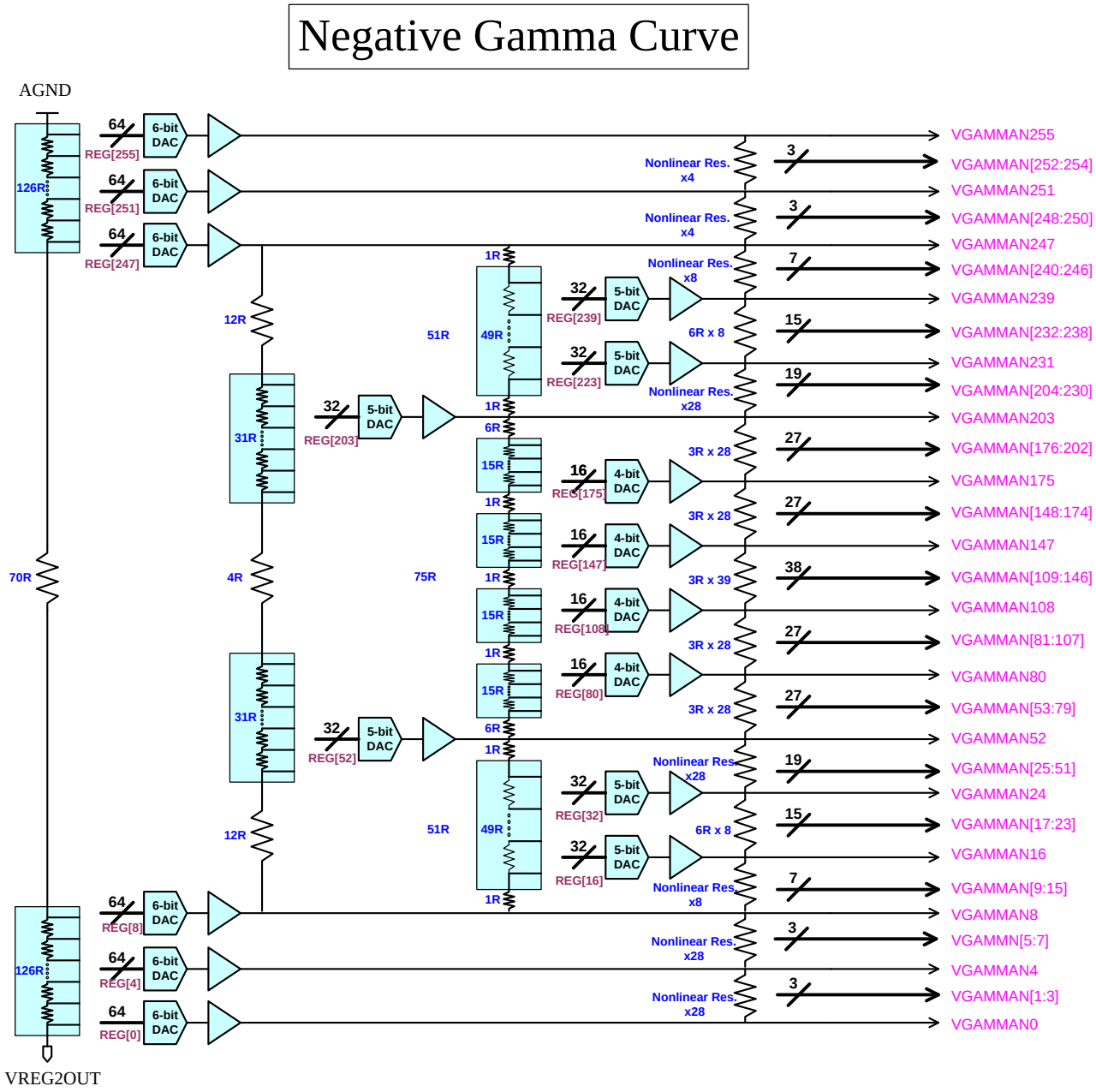


Figure 105 Negative Gamma Control (Page1_C0h~CFh)

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Positive polarity	Resister stream	Gamma 256 grayscale voltage calculation formula
VGAMMAP0	0R	AGND+ΔVDHP(322R-2R*VP0[5:0])/322R , ΔVDHP=(VREG1OUT-AGND)
VGAMMAP1	21R	VGAMMAP4+(VGAMMP0-VGAMMAP4)*(57R)/(78R)
VGAMMAP2	21R	VGAMMAP4+(VGAMMP0-VGAMMAP4)*(36R)/(78R)
VGAMMAP3	18R	VGAMMAP4+(VGAMMP0-VGAMMAP4)*(18R)/(78R)
VGAMMAP4	18R	AGND+ΔVDHP(322R-2R*VP4[5:0])/322R , ΔVDHP=(VREG1OUT-AGND)
VGAMMAP5	30R	VGAMMAP8+((VGAMMAP4-VGAMMAP8)*(90R/120R)
VGAMMAP6	30R	VGAMMAP8+((VGAMMAP4-VGAMMAP8)*(60R/120R)
VGAMMAP7	30R	VGAMMAP8+((VGAMMAP4-VGAMMAP8)*(30R/120R)
VGAMMAP8	30R	AGND+ΔVDHP(322R-2R*VP8[5:0])/322R , ΔVDHP=(VREG1OUT-AGND)
VGAMMAP9	24R	VGAMMAP16+((VGAMMAP8-VGAMMAP16)*(136R/160R)
VGAMMAP10	22R	VGAMMAP16+((VGAMMAP8-VGAMMAP16)*(114R/160R)
VGAMMAP11	20R	VGAMMAP16+((VGAMMAP8-VGAMMAP16)*(94R/160R)
VGAMMAP12	20R	VGAMMAP16+((VGAMMAP8-VGAMMAP16)*(74R/160R)
VGAMMAP13	20R	VGAMMAP16+((VGAMMAP8-VGAMMAP16)*(54R/160R)
VGAMMAP14	18R	VGAMMAP16+((VGAMMAP8-VGAMMAP16)*(36R/160R)
VGAMMAP15	18R	VGAMMAP16+((VGAMMAP8-VGAMMAP16)*(18R/160R)
VGAMMAP16	18R	VGAMMAP52+(VGAMMAP8-VGAMMAP52)*((50R-1R*VP16[4:0])/51R)
VGAMMAP17	12R	VGAMMAP24+((VGAMMAP16-VGAMMAP24)*(84R/96R)
VGAMMAP18	12R	VGAMMAP24+((VGAMMAP16-VGAMMAP24)*(72R/96R)
VGAMMAP19	12R	VGAMMAP24+((VGAMMAP16-VGAMMAP24)*(60R/96R)
VGAMMAP20	12R	VGAMMAP24+((VGAMMAP16-VGAMMAP24)*(48R/96R)
VGAMMAP21	12R	VGAMMAP24+((VGAMMAP16-VGAMMAP24)*(36R/96R)
VGAMMAP22	12R	VGAMMAP24+((VGAMMAP16-VGAMMAP24)*(24R/96R)
VGAMMAP23	12R	VGAMMAP24+((VGAMMAP16-VGAMMAP24)*(12R/96R)
VGAMMAP24	12R	VGAMMAP52+(VGAMMAP8-VGAMMAP52)*((32R-1R*VP24[4:0])/51R)
VGAMMAP25	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(268R/280R)
VGAMMAP26	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(256R/280R)
VGAMMAP27	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(244R/280R)
VGAMMAP28	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(232R/280R)
VGAMMAP29	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(220R/280R)
VGAMMAP30	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(208R/280R)
VGAMMAP31	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(196R/280R)
VGAMMAP31	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(184R/280R)
VGAMMAP33	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(174R/280R)
VGAMMAP34	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(164R/280R)
VGAMMAP35	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(154R/280R)

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VGAMMAP36	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(144R/280R)
VGAMMAP31	12R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(134R/280R)
VGAMMAP38	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(124R/280R)
VGAMMAP39	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(114R/280R)
VGAMMAP40	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(104R/280R)
VGAMMAP41	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(94R/280R)
VGAMMAP42	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(84R/280R)
VGAMMAP43	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(74R/280R)
VGAMMAP44	10R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(64R/280R)
VGAMMAP45	8R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(56R/280R)
VGAMMAP46	8R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(48R/280R)
VGAMMAP47	8R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(40R/280R)
VGAMMAP48	8R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(32R/280R)
VGAMMAP49	8R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(24R/280R)
VGAMMAP50	8R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(16R/280R)
VGAMMAP51	8R	VGAMMAP52+((VGAMMAP24-VGAMMAP52)*(8R/280R)
VGAMMAP52	8R	VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((77R-0R)/90R)) , VP52[4:0] =0(Dec) VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((77R-2R)/90R)) , VP52[4:0] =1(Dec) VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((77R-4R)/90R)) , VP52[4:0] =2(Dec) VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((74R-1R*VP52[4:0])/90R)) , else
VGAMMAP53	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(81R/84R)
VGAMMAP54	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(78R/84R)
VGAMMAP55	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(75R/84R)
VGAMMAP56	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(72R/84R)
VGAMMAP57	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(69R/84R)
VGAMMAP58	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(66R/84R)
VGAMMAP59	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(63R/84R)
VGAMMAP60	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(60R/84R)
VGAMMAP61	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(57R/84R)
VGAMMAP62	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(54R/84R)
VGAMMAP63	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(51R/84R)
VGAMMAP64	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(48R/84R)
VGAMMAP65	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(45R/84R)
VGAMMAP66	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(42R/84R)
VGAMMAP67	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(39R/84R)
VGAMMAP68	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(36R/84R)
VGAMMAP69	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(33R/84R)

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VGAMMAP70	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(30R/84R)
VGAMMAP71	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(27R/84R)
VGAMMAP72	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(24R/84R)
VGAMMAP73	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(21R/84R)
VGAMMAP74	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(18R/84R)
VGAMMAP75	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(15R/84R)
VGAMMAP76	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(12R/84R)
VGAMMAP77	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(9R/84R)
VGAMMAP78	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(6R/84R)
VGAMMAP79	4R	VGAMMAP80+((VGAMMAP52-VGAMMAP80)*(3R/84R)
VGAMMAP80	4R	VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((68R-0R)/75R) , VP80[3:0] =0(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((68R-2R)/75R) , VP80[3:0] =1(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((68R-4R)/75R) , VP80[3:0] =2(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((65R-1R*VP80[3:0])/75R) , else
VGAMMAP81	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(81R+/84R)
VGAMMAP82	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(78R/84R)
VGAMMAP83	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(75R/84R)
VGAMMAP84	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(72R/84R)
VGAMMAP85	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(69R/84R)
VGAMMAP86	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(66R/84R)
VGAMMAP87	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(63R/84R)
VGAMMAP88	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(60R/84R)
VGAMMAP89	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(57R/84R)
VGAMMAP90	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(54R/84R)
VGAMMAP91	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(51R/84R)
VGAMMAP92	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(48R/84R)
VGAMMAP93	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(45R/84R)
VGAMMAP94	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(42R/84R)
VGAMMAP95	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(39R/84R)
VGAMMAP96	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(36R/84R)
VGAMMAP97	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(33R/84R)
VGAMMAP98	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(30R/84R)
VGAMMAP99	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(27R/84R)
VGAMMAP100	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(24R/84R)
VGAMMAP101	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(21R/84R)
VGAMMAP102	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(18R/84R)
VGAMMAP103	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(15R/84R)

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VGAMMAP104	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(12R/84R)
VGAMMAP105	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(9R/84R)
VGAMMAP106	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(6R/84R)
VGAMMAP107	4R	VGAMMAP108+((VGAMMAP80-VGAMMAP108)*(3R/84R)
VGAMMAP108	4R	VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((52R-0R/75R) , VP108[3:0] =0(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((52R-2R/75R) , VP108[3:0] =1(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((52R-4R/75R) , VP108[3:0] =2(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((49R-1R*VP108[3:0])/75R) , else
VGAMMAP109	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(114R/117R)
VGAMMAP110	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(111R/117R)
VGAMMAP111	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(108R/117R)
VGAMMAP112	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(105R/117R)
VGAMMAP113	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(102R/117R)
VGAMMAP114	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(99R/117R)
VGAMMAP115	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(96R/117R)
VGAMMAP116	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(93R/117R)
VGAMMAP117	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(90R/117R)
VGAMMAP118	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(87R/117R)
VGAMMAP119	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(84R/117R)
VGAMMAP120	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(81R/117R)
VGAMMAP121	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(78R/117R)
VGAMMAP122	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(75R/117R)
VGAMMAP123	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(72R/117R)
VGAMMAP124	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(69R/117R)
VGAMMAP125	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(66R/117R)
VGAMMAP126	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(63R/117R)
VGAMMAP127	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(60R/117R)
VGAMMAP128	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(57R/117R)
VGAMMAP129	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(54R/117R)
VGAMMAP130	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(51R/117R)
VGAMMAP131	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(48R/117R)
VGAMMAP132	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(45R/117R)
VGAMMAP133	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(42R/117R)
VGAMMAP134	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(39R/117R)
VGAMMAP135	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(36R/117R)
VGAMMAP136	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(33R/117R)
VGAMMAP137	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(30R/117R)

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VGAMMAP138	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(27R/117R)
VGAMMAP139	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(24R/117R)
VGAMMAP140	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(21R/117R)
VGAMMAP141	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(18R/117R)
VGAMMAP142	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(15R/117R)
VGAMMAP143	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(12R/117R)
VGAMMAP144	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(9R/117R)
VGAMMAP145	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(6R/117R)
VGAMMAP146	4R	VGAMMAP147+((VGAMMAP108-VGAMMAP147)*(3R/117R)
VGAMMAP147	4R	VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((17R+1R*VP147[3:0])/75R) , else VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((17R+31R/75R) , VP147[3:0] =13(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((17R+33R/75R) , VP147[3:0] =14(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((17R+35R/75R) , VP147[3:0] =15(Dec)
VGAMMAP148	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(81R/84R)
VGAMMAP149	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(78R/84R)
VGAMMAP150	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(75R/84R)
VGAMMAP151	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(72R/84R)
VGAMMAP152	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(69R/84R)
VGAMMAP153	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(66R/84R)
VGAMMAP154	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(63R/84R)
VGAMMAP155	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(60R/84R)
VGAMMAP156	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(57R/84R)
VGAMMAP157	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(54R/84R)
VGAMMAP158	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(51R/84R)
VGAMMAP159	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(48R/84R)
VGAMMAP160	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(45R/84R)
VGAMMAP161	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(42R/84R)
VGAMMAP162	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(39R/84R)
VGAMMAP163	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(36R/84R)
VGAMMAP164	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(33R/84R)
VGAMMAP165	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(30R/84R)
VGAMMAP166	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(27R/84R)
VGAMMAP167	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(24R/84R)
VGAMMAP168	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(21R/84R)
VGAMMAP169	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(18R/84R)
VGAMMAP170	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(15R/84R)
VGAMMAP171	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(12R/84R)

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VGAMMAP172	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(9R/84R)
VGAMMAP173	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(6R/84R)
VGAMMAP174	4R	VGAMMAP175+((VGAMMAP147-VGAMMAP175)*(3R/84R)
VGAMMAP175	4R	VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((1R+1R*VP175[3:0])/75R) , else VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((1R+15R/75R) , VP175[3:0] =13(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((1R+17R/75R) , VP175[3:0] =14(Dec) VGAMMAP203+(VGAMMAP52-VGAMMAP203)*((1R+19R/75R) , VP175[3:0] =15(Dec)
VGAMMAP176	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(81R/84R)
VGAMMAP177	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(78R/84R)
VGAMMAP178	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(75R/84R)
VGAMMAP179	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(72R/84R)
VGAMMAP180	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(69R/84R)
VGAMMAP181	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(66R/84R)
VGAMMAP182	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(63R/84R)
VGAMMAP183	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(60R/84R)
VGAMMAP184	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(57R/84R)
VGAMMAP185	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(54R/84R)
VGAMMAP186	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(51R/84R)
VGAMMAP187	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(48R/84R)
VGAMMAP188	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(45R/84R)
VGAMMAP189	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(42R/84R)
VGAMMAP190	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(39R/84R)
VGAMMAP191	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(36R/84R)
VGAMMAP192	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(33R/84R)
VGAMMAP193	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(30R/84R)
VGAMMAP194	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(27R/84R)
VGAMMAP195	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(24R/84R)
VGAMMAP196	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(21R/84R)
VGAMMAP197	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(18R/84R)
VGAMMAP198	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(15R/84R)
VGAMMAP199	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(12R/84R)
VGAMMAP200	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(9R/84R)
VGAMMAP201	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(6R/84R)
VGAMMAP202	4R	VGAMMAP203+((VGAMMAP175-VGAMMAP203)*(3R/84R)
VGAMMAP203	4R	VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((8R+1R*VP203[4:0])/90R)) , else VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((8R+38R/90R)) , VP203[4:0] =29(Dec) VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((8R+40R/90R)) , VP203[4:0] =30(Dec)

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		VGAMMAP247+(VGAMMAP8-VGAMMAP247)*((8R+42R/90R)) , VP203[4:0] =31(Dec)
VGAMMAP204	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(136R/140R)
VGAMMAP205	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(132R/140R)
VGAMMAP206	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(128R/140R)
VGAMMAP207	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(124R/140R)
VGAMMAP208	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(120R/140R)
VGAMMAP209	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(116R/140R)
VGAMMAP210	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(112R/140R)
VGAMMAP211	4R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(108R/140R)
VGAMMAP212	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(103R/140R)
VGAMMAP213	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(98R/140R)
VGAMMAP214	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(93R/140R)
VGAMMAP215	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(88R/140R)
VGAMMAP216	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(83R/140R)
VGAMMAP217	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(78R/140R)
VGAMMAP218	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(73R/140R)
VGAMMAP219	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(68R/140R)
VGAMMAP220	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(63R/140R)
VGAMMAP221	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(58R/140R)
VGAMMAP222	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(53R/140R)
VGAMMAP223	5R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(48R/140R)
VGAMMAP224	6R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(42R/140R)
VGAMMAP225	6R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(36R/140R)
VGAMMAP226	6R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(30R/140R)
VGAMMAP227	6R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(24R/140R)
VGAMMAP228	6R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(18R/140R)
VGAMMAP229	6R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(12R/140R)
VGAMMAP230	6R	VGAMMAP231+((VGAMMAP203-VGAMMAP231)*(6R/140R)
VGAMMAP231	6R	VGAMMAP247+(VGAMMAP203-VGAMMAP247)*((1R+1R*VP231[4:0])/51R)
VGAMMAP232	6R	VGAMMAP239+((VGAMMAP231-VGAMMAP239)*(42R/48R)
VGAMMAP233	6R	VGAMMAP239+((VGAMMAP231-VGAMMAP239)*(36R/48R)
VGAMMAP234	6R	VGAMMAP239+((VGAMMAP231-VGAMMAP239)*(30R/48R)
VGAMMAP235	6R	VGAMMAP239+((VGAMMAP231-VGAMMAP239)*(24R/48R)
VGAMMAP236	6R	VGAMMAP239+((VGAMMAP231-VGAMMAP239)*(18R/48R)
VGAMMAP237	6R	VGAMMAP239+((VGAMMAP231-VGAMMAP239)*(12R/48R)
VGAMMAP238	6R	VGAMMAP239+((VGAMMAP231-VGAMMAP239)*(6R/48R)
VGAMMAP239	15R	VGAMMAP247+(VGAMMAP203-VGAMMAP247)*((1R+1R*VP239[4:0])/51R)

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VGAMMAP240	6R	VGAMMAP247+((VGAMMAP239-VGAMMAP247)*(74R/80R)
VGAMMAP241	7R	VGAMMAP247+((VGAMMAP239-VGAMMAP247)*(67R/80R)
VGAMMAP242	9R	VGAMMAP247+((VGAMMAP239-VGAMMAP247)*(58R/80R)
VGAMMAP243	8R	VGAMMAP247+((VGAMMAP239-VGAMMAP247)*(50R/80R)
VGAMMAP244	11R	VGAMMAP247+((VGAMMAP239-VGAMMAP247)*(39R/80R)
VGAMMAP245	12R	VGAMMAP247+((VGAMMAP239-VGAMMAP247)*(27R/80R)
VGAMMAP246	12R	VGAMMAP247+((VGAMMAP239-VGAMMAP247)*(15R/80R)
VGAMMAP247	15R	AGND+ΔVDHP(3R*VP247[5:0])/322R , ΔVDHP=(VREG1OUT-AGND)
VGAMMAP248	12R	VGAMMAP251+((VGAMMAP247-VGAMMAP251)*(68R/80R)
VGAMMAP249	16R	VGAMMAP251+((VGAMMAP247-VGAMMAP251)*(52R/80R)
VGAMMAP250	24R	VGAMMAP251+((VGAMMAP247-VGAMMAP251)*(28R/80R)
VGAMMAP251	28R	AGND+ΔVDHP(3R*VP251[5:0])/322R , ΔVDHP=(VREG1OUT-AGND)
VGAMMAP252	25R	VGAMMAP255+(VGAMMP251-VGAMMAP255)*(105R/130R)
VGAMMAP253	45R	VGAMMAP255+(VGAMMP251-VGAMMAP255)*(60R/130R)
VGAMMAP254	20R	VGAMMAP255+(VGAMMP251-VGAMMAP255)*(40R/130R)
VGAMMAP255	10R	AGND+ΔVDHP(3R*VP255[5:0])/322R , ΔVDHP=(VREG1OUT-AGND)

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Negative polarity	Resister stream	Gamma 256 grayscale voltage calculation formula
VGAMMAN0	0R	AGND+ΔVDHN(322R-2R*VN0[5:0])/322R , ΔVDHN=(VREG2OUT-AGND)
VGAMMAN1	21R	VGAMMAN4+(VGAMMN0-VGAMMAN4)*(57R)/(78R)
VGAMMAN2	21R	VGAMMAN4+(VGAMMN0-VGAMMAN4)*(36R)/(78R)
VGAMMAN3	18R	VGAMMAN4+(VGAMMN0-VGAMMAN4)*(18R)/(78R)
VGAMMAN4	18R	AGND+ΔVDHN(322R-2R*VN4[5:0])/322R , ΔVDHN=(VREG2OUT-AGND)
VGAMMAN5	30R	VGAMMAN8+((VGAMMAN4-VGAMMAN8)*(90R/120R)
VGAMMAN6	30R	VGAMMAN8+((VGAMMAN4-VGAMMAN8)*(60R/120R)
VGAMMAN7	30R	VGAMMAN8+((VGAMMAN4-VGAMMAN8)*(30R/120R)
VGAMMAN8	30R	AGND+ΔVDHN(322R-2R*VN8[5:0])/322R , ΔVDHN=(VREG2OUT-AGND)
VGAMMAN9	24R	VGAMMAN16+((VGAMMAN8-VGAMMAN16)*(136R/160R)
VGAMMAN10	22R	VGAMMAN16+((VGAMMAN8-VGAMMAN16)*(114R/160R)
VGAMMAN11	20R	VGAMMAN16+((VGAMMAN8-VGAMMAN16)*(94R/160R)
VGAMMAN12	20R	VGAMMAN16+((VGAMMAN8-VGAMMAN16)*(74R/160R)
VGAMMAN13	20R	VGAMMAN16+((VGAMMAN8-VGAMMAN16)*(54R/160R)
VGAMMAN14	18R	VGAMMAN16+((VGAMMAN8-VGAMMAN16)*(36R/160R)
VGAMMAN15	18R	VGAMMAN16+((VGAMMAN8-VGAMMAN16)*(18R/160R)
VGAMMAN16	18R	VGAMMAN52+(VGAMMAN8-VGAMMAN52)*((50R-1R*VN16[4:0])/51R)
VGAMMAN17	12R	VGAMMAN24+((VGAMMAN16-VGAMMAN24)*(84R/96R)
VGAMMAN18	12R	VGAMMAN24+((VGAMMAN16-VGAMMAN24)*(72R/96R)
VGAMMAN19	12R	VGAMMAN24+((VGAMMAN16-VGAMMAN24)*(60R/96R)
VGAMMAN20	12R	VGAMMAN24+((VGAMMAN16-VGAMMAN24)*(48R/96R)
VGAMMAN21	12R	VGAMMAN24+((VGAMMAN16-VGAMMAN24)*(36R/96R)
VGAMMAN22	12R	VGAMMAN24+((VGAMMAN16-VGAMMAN24)*(24R/96R)
VGAMMAN23	12R	VGAMMAN24+((VGAMMAN16-VGAMMAN24)*(12R/96R)
VGAMMAN24	12R	VGAMMAN52+(VGAMMAN8-VGAMMAN52)*((32R-1R*VN24[4:0])/51R)
VGAMMAN25	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(268R/280R)
VGAMMAN26	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(256R/280R)
VGAMMAN27	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(244R/280R)
VGAMMAN28	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(232R/280R)
VGAMMAN29	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(220R/280R)
VGAMMAN30	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(208R/280R)
VGAMMAN31	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(196R/280R)
VGAMMAN31	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(184R/280R)
VGAMMAN33	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(174R/280R)
VGAMMAN34	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(164R/280R)

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VGAMMAN35	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(154R/280R)
VGAMMAN36	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(144R/280R)
VGAMMAN31	12R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(134R/280R)
VGAMMAN38	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(124R/280R)
VGAMMAN39	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(114R/280R)
VGAMMAN40	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(104R/280R)
VGAMMAN41	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(94R/280R)
VGAMMAN42	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(84R/280R)
VGAMMAN43	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(74R/280R)
VGAMMAN44	10R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(64R/280R)
VGAMMAN45	8R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(56R/280R)
VGAMMAN46	8R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(48R/280R)
VGAMMAN47	8R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(40R/280R)
VGAMMAN48	8R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(32R/280R)
VGAMMAN49	8R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(24R/280R)
VGAMMAN50	8R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(16R/280R)
VGAMMAN51	8R	VGAMMAN52+((VGAMMAN24-VGAMMAN52)*(8R/280R)
VGAMMAN52	8R	VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((77R-0R)/90R)) , VN52[4:0] =0(Dec) VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((77R-2R)/90R)) , VN52[4:0] =1(Dec) VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((77R-4R)/90R)) , VN52[4:0] =2(Dec) VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((74R-1R*VN52[4:0])/90R)) , else
VGAMMAN53	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(81R/84R)
VGAMMAN54	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(78R/84R)
VGAMMAN55	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(75R/84R)
VGAMMAN56	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(72R/84R)
VGAMMAN57	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(69R/84R)
VGAMMAN58	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(66R/84R)
VGAMMAN59	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(63R/84R)
VGAMMAN60	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(60R/84R)
VGAMMAN61	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(57R/84R)
VGAMMAN62	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(54R/84R)
VGAMMAN63	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(51R/84R)
VGAMMAN64	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(48R/84R)
VGAMMAN65	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(45R/84R)
VGAMMAN66	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(42R/84R)
VGAMMAN67	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(39R/84R)
VGAMMAN68	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(36R/84R)

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VGAMMAN69	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(33R/84R)
VGAMMAN70	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(30R/84R)
VGAMMAN71	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(27R/84R)
VGAMMAN72	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(24R/84R)
VGAMMAN73	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(21R/84R)
VGAMMAN74	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(18R/84R)
VGAMMAN75	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(15R/84R)
VGAMMAN76	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(12R/84R)
VGAMMAN77	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(9R/84R)
VGAMMAN78	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(6R/84R)
VGAMMAN79	4R	VGAMMAN80+((VGAMMAN52-VGAMMAN80)*(3R/84R)
VGAMMAN80	4R	VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((68R-0R)/75R) , VN80[3:0] =0(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((68R-2R)/75R) , VN80[3:0] =1(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((68R-4R)/75R) , VN80[3:0] =2(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((65R-1R*VN80[3:0])/75R) , else
VGAMMAN81	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(81R+/84R)
VGAMMAN82	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(78R/84R)
VGAMMAN83	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(75R/84R)
VGAMMAN84	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(72R/84R)
VGAMMAN85	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(69R/84R)
VGAMMAN86	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(66R/84R)
VGAMMAN87	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(63R/84R)
VGAMMAN88	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(60R/84R)
VGAMMAN89	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(57R/84R)
VGAMMAN90	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(54R/84R)
VGAMMAN91	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(51R/84R)
VGAMMAN92	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(48R/84R)
VGAMMAN93	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(45R/84R)
VGAMMAN94	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(42R/84R)
VGAMMAN95	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(39R/84R)
VGAMMAN96	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(36R/84R)
VGAMMAN97	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(33R/84R)
VGAMMAN98	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(30R/84R)
VGAMMAN99	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(27R/84R)
VGAMMAN100	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(24R/84R)
VGAMMAN101	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(21R/84R)
VGAMMAN102	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(18R/84R)

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VGAMMAN103	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(15R/84R)
VGAMMAN104	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(12R/84R)
VGAMMAN105	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(9R/84R)
VGAMMAN106	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(6R/84R)
VGAMMAN107	4R	VGAMMAN108+((VGAMMAN80-VGAMMAN108)*(3R/84R)
VGAMMAN108	4R	VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((52R-0R/75R) , VN108[3:0] =0(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((52R-2R/75R) , VN108[3:0] =1(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((52R-4R/75R) , VN108[3:0] =2(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((49R-1R*VN108[3:0])/75R) , else
VGAMMAN109	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(114R/117R)
VGAMMAN110	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(111R/117R)
VGAMMAN111	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(108R/117R)
VGAMMAN112	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(105R/117R)
VGAMMAN113	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(102R/117R)
VGAMMAN114	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(99R/117R)
VGAMMAN115	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(96R/117R)
VGAMMAN116	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(93R/117R)
VGAMMAN117	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(90R/117R)
VGAMMAN118	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(87R/117R)
VGAMMAN119	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(84R/117R)
VGAMMAN120	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(81R/117R)
VGAMMAN121	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(78R/117R)
VGAMMAN122	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(75R/117R)
VGAMMAN123	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(72R/117R)
VGAMMAN124	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(69R/117R)
VGAMMAN125	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(66R/117R)
VGAMMAN126	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(63R/117R)
VGAMMAN127	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(60R/117R)
VGAMMAN128	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(57R/117R)
VGAMMAN129	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(54R/117R)
VGAMMAN130	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(51R/117R)
VGAMMAN131	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(48R/117R)
VGAMMAN132	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(45R/117R)
VGAMMAN133	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(42R/117R)
VGAMMAN134	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(39R/117R)
VGAMMAN135	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(36R/117R)
VGAMMAN136	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(33R/117R)

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VGAMMAN137	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(30R/117R)
VGAMMAN138	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(27R/117R)
VGAMMAN139	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(24R/117R)
VGAMMAN140	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(21R/117R)
VGAMMAN141	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(18R/117R)
VGAMMAN142	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(15R/117R)
VGAMMAN143	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(12R/117R)
VGAMMAN144	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(9R/117R)
VGAMMAN145	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(6R/117R)
VGAMMAN146	4R	VGAMMAN147+((VGAMMAN108-VGAMMAN147)*(3R/117R)
VGAMMAN147	4R	VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((17R+1R*VN147[3:0])/75R) , else VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((17R+31R/75R) , VN147[3:0] =13(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((17R+33R/75R) , VN147[3:0] =14(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((17R+35R/75R) , VN147[3:0] =15(Dec)
VGAMMAN148	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(81R/84R)
VGAMMAN149	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(78R/84R)
VGAMMAN150	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(75R/84R)
VGAMMAN151	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(72R/84R)
VGAMMAN152	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(69R/84R)
VGAMMAN153	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(66R/84R)
VGAMMAN154	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(63R/84R)
VGAMMAN155	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(60R/84R)
VGAMMAN156	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(57R/84R)
VGAMMAN157	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(54R/84R)
VGAMMAN158	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(51R/84R)
VGAMMAN159	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(48R/84R)
VGAMMAN160	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(45R/84R)
VGAMMAN161	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(42R/84R)
VGAMMAN162	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(39R/84R)
VGAMMAN163	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(36R/84R)
VGAMMAN164	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(33R/84R)
VGAMMAN165	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(30R/84R)
VGAMMAN166	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(27R/84R)
VGAMMAN167	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(24R/84R)
VGAMMAN168	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(21R/84R)
VGAMMAN169	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(18R/84R)
VGAMMAN170	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(15R/84R)

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VGAMMAN171	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(12R/84R)
VGAMMAN172	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(9R/84R)
VGAMMAN173	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(6R/84R)
VGAMMAN174	4R	VGAMMAN175+((VGAMMAN147-VGAMMAN175)*(3R/84R)
VGAMMAN175	4R	VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((1R+1R*VN175[3:0])/75R) , else VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((1R+15R/75R) , VN175[3:0] =13(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((1R+17R/75R) , VN175[3:0] =14(Dec) VGAMMAN203+(VGAMMAN52-VGAMMAN203)*((1R+19R/75R) , VN175[3:0] =15(Dec)
VGAMMAN176	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(81R/84R)
VGAMMAN177	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(78R/84R)
VGAMMAN178	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(75R/84R)
VGAMMAN179	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(72R/84R)
VGAMMAN180	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(69R/84R)
VGAMMAN181	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(66R/84R)
VGAMMAN182	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(63R/84R)
VGAMMAN183	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(60R/84R)
VGAMMAN184	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(57R/84R)
VGAMMAN185	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(54R/84R)
VGAMMAN186	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(51R/84R)
VGAMMAN187	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(48R/84R)
VGAMMAN188	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(45R/84R)
VGAMMAN189	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(42R/84R)
VGAMMAN190	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(39R/84R)
VGAMMAN191	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(36R/84R)
VGAMMAN192	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(33R/84R)
VGAMMAN193	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(30R/84R)
VGAMMAN194	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(27R/84R)
VGAMMAN195	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(24R/84R)
VGAMMAN196	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(21R/84R)
VGAMMAN197	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(18R/84R)
VGAMMAN198	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(15R/84R)
VGAMMAN199	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(12R/84R)
VGAMMAN200	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(9R/84R)
VGAMMAN201	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(6R/84R)
VGAMMAN202	4R	VGAMMAN203+((VGAMMAN175-VGAMMAN203)*(3R/84R)
VGAMMAN203	4R	VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((8R+1R*VN203[4:0])/90R)) , else VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((8R+38R/90R)) , VN203[4:0] =29(Dec)

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		VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((8R+40R/90R)) , VN203[4:0] =30(Dec) VGAMMAN247+(VGAMMAN8-VGAMMAN247)*((8R+42R/90R)) , VN203[4:0] =31(Dec)
VGAMMAN204	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(136R/140R)
VGAMMAN205	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(132R/140R)
VGAMMAN206	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(128R/140R)
VGAMMAN207	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(124R/140R)
VGAMMAN208	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(120R/140R)
VGAMMAN209	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(116R/140R)
VGAMMAN210	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(112R/140R)
VGAMMAN211	4R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(108R/140R)
VGAMMAN212	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(103R/140R)
VGAMMAN213	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(98R/140R)
VGAMMAN214	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(93R/140R)
VGAMMAN215	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(88R/140R)
VGAMMAN216	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(83R/140R)
VGAMMAN217	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(78R/140R)
VGAMMAN218	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(73R/140R)
VGAMMAN219	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(68R/140R)
VGAMMAN220	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(63R/140R)
VGAMMAN221	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(58R/140R)
VGAMMAN222	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(53R/140R)
VGAMMAN223	5R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(48R/140R)
VGAMMAN224	6R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(42R/140R)
VGAMMAN225	6R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(36R/140R)
VGAMMAN226	6R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(30R/140R)
VGAMMAN227	6R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(24R/140R)
VGAMMAN228	6R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(18R/140R)
VGAMMAN229	6R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(12R/140R)
VGAMMAN230	6R	VGAMMAN231+((VGAMMAN203-VGAMMAN231)*(6R/140R)
VGAMMAN231	6R	VGAMMAN247+(VGAMMAN203-VGAMMAN247)*((1R+1R*VN231[4:0])/51R)
VGAMMAN232	6R	VGAMMAN239+((VGAMMAN231-VGAMMAN239)*(42R/48R)
VGAMMAN233	6R	VGAMMAN239+((VGAMMAN231-VGAMMAN239)*(36R/48R)
VGAMMAN234	6R	VGAMMAN239+((VGAMMAN231-VGAMMAN239)*(30R/48R)
VGAMMAN235	6R	VGAMMAN239+((VGAMMAN231-VGAMMAN239)*(24R/48R)
VGAMMAN236	6R	VGAMMAN239+((VGAMMAN231-VGAMMAN239)*(18R/48R)
VGAMMAN237	6R	VGAMMAN239+((VGAMMAN231-VGAMMAN239)*(12R/48R)
VGAMMAN238	6R	VGAMMAN239+((VGAMMAN231-VGAMMAN239)*(6R/48R)

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VGAMMAN239	15R	VGAMMAN247+(VGAMMAN203-VGAMMAN247)*((1R+1R*VN239[4:0])/51R)
VGAMMAN240	6R	VGAMMAN247+((VGAMMAN239-VGAMMAN247)*(74R/80R)
VGAMMAN241	7R	VGAMMAN247+((VGAMMAN239-VGAMMAN247)*(67R/80R)
VGAMMAN242	9R	VGAMMAN247+((VGAMMAN239-VGAMMAN247)*(58R/80R)
VGAMMAN243	8R	VGAMMAN247+((VGAMMAN239-VGAMMAN247)*(50R/80R)
VGAMMAN244	11R	VGAMMAN247+((VGAMMAN239-VGAMMAN247)*(39R/80R)
VGAMMAN245	12R	VGAMMAN247+((VGAMMAN239-VGAMMAN247)*(27R/80R)
VGAMMAN246	12R	VGAMMAN247+((VGAMMAN239-VGAMMAN247)*(15R/80R)
VGAMMAN247	15R	AGND+ΔVDHN(3R*VN247[5:0])/322R , ΔVDHN=(VREG2OUT-AGND)
VGAMMAN248	12R	VGAMMAN251+((VGAMMAN247-VGAMMAN251)*(68R/80R)
VGAMMAN249	16R	VGAMMAN251+((VGAMMAN247-VGAMMAN251)*(52R/80R)
VGAMMAN250	24R	VGAMMAN251+((VGAMMAN247-VGAMMAN251)*(28R/80R)
VGAMMAN251	28R	AGND+ΔVDHN(3R*VN251[5:0])/322R , ΔVDHN=(VREG2OUT-AGND)
VGAMMAN252	25R	VGAMMAN255+(VGAMMN251-VGAMMAN255)*(105R/130R)
VGAMMAN253	45R	VGAMMAN255+(VGAMMN251-VGAMMAN255)*(60R/130R)
VGAMMAN254	20R	VGAMMAN255+(VGAMMN251-VGAMMAN255)*(40R/130R)
VGAMMAN255	10R	AGND+ΔVDHN(3R*VN255[5:0])/322R , ΔVDHN=(VREG2OUT-AGND)

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11. Deep Standby Mode

11.1. Deep Standby Entry/Exit Sequence Flow Chart

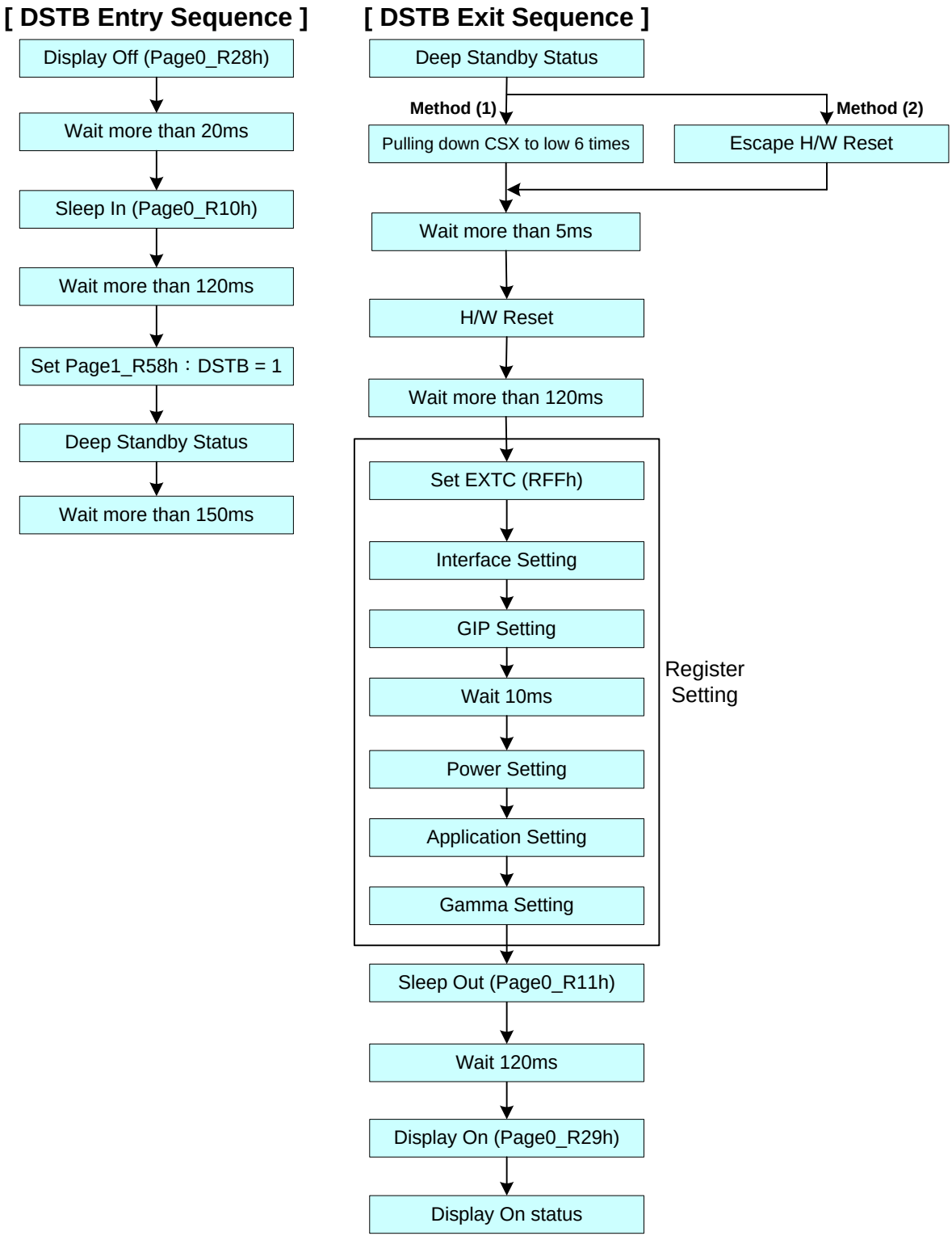


Figure 106: Deep Standby Entry/Exit Sequence Flow Chart

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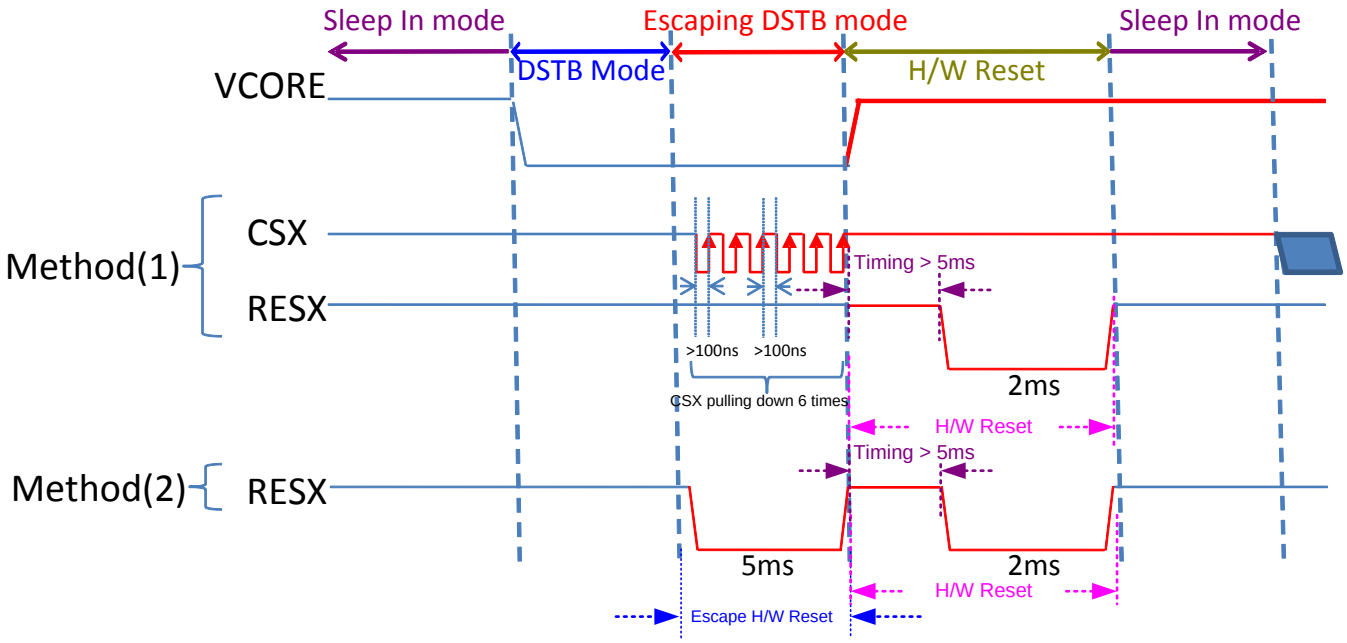


Figure 107: CSX/RESX protocol for escaping DSTB mode

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11.2. Deep Standby Mode Setting

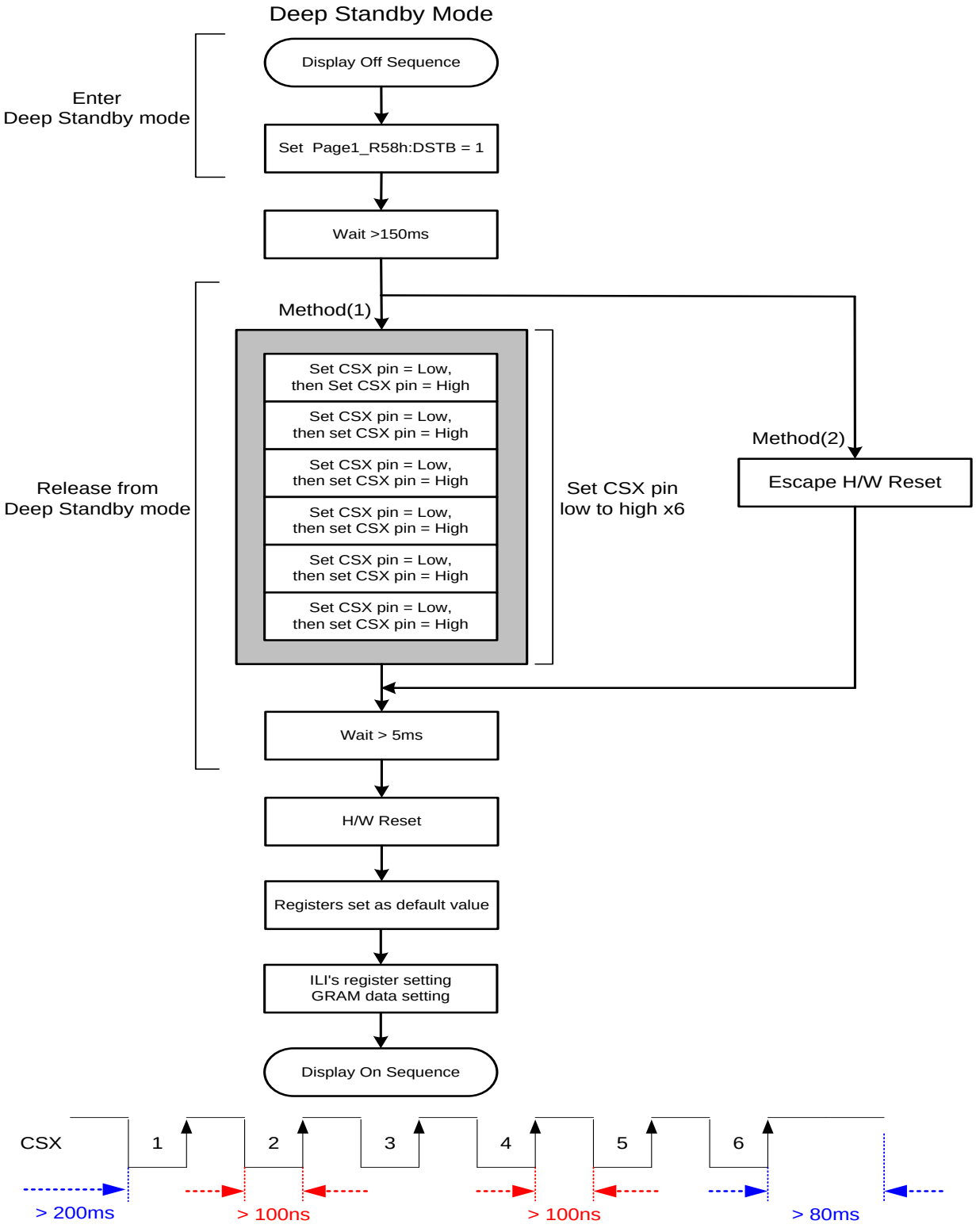


Figure 108 Deep Standby Mode Entry / Exit

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12. Synchronization Time

The GPO[3:2] of ILI9806E-2C can output the synchronization signals to touch sensing signal for touch panel controller. To use these signals, touch panel controller can receive touch sensing signal while avoiding display changing noise.

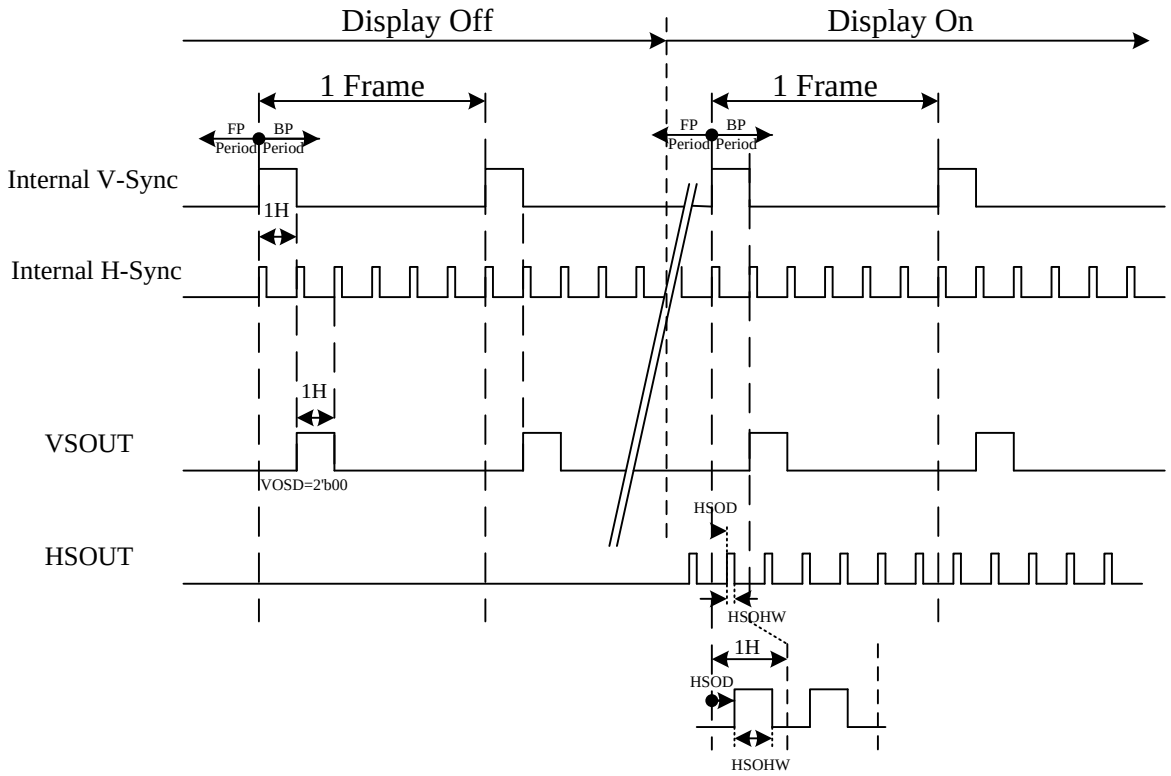
These signals are consist of vertical synchronization signal: VSOUT and horizontal synchronization signal: HSOUT. The level of output voltage is IOVCC to GND. Each signal can adjust output timing for internal synchronization signal. The high level width of VSOUT is 1 line, and it is adjustable.VSOUT is outputted always, but HSOUT is outputted during displaying only.

(1) VSOUT output Timing

VSOUT output means internal VSYNC is starting point. VSOUT output timing can be adjusted by VSOD register. Unit is 1H.

(2) HSOUT output Timing

HSOUT output means internal source output timing is starting point. HSOUT output timing can be adjusted by HSOD register. And HSOUT high level width can be adjusted by HSOHW register.



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13. Electrical Characteristics

13.1. Absolute Maximum Ratings

The absolute maximum rating is listed on Table 43. When the ILI9806E-2C is used out of the absolute maximum ratings, it may be permanently damaged. To use the ILI9806E-2C within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9806E-2C will malfunction and cause poor reliability.

Table 43 Absolute Maximum Ratings

Item	Symbol	Unit	Value
Supply voltage(Analog)	VCI ~ AGND	V	-0.3 ~ +4.6
Supply voltage(Analog)	VCIP ~ CGND	V	-0.3 ~ +4.6
Supply voltage(Analog)	VCIR ~ VSSR1	V	-0.3 ~ +4.6
Supply voltage (I/O)	IOVCC ~ DGND	V	-0.3 ~ +4.6
OTP Supply voltage	VPP ~ AGND	V	-0.3 ~ +6.6
Supply voltage	DDVDH ~ AGND	V	-0.3 ~ +6.6
Supply voltage	DDVDL ~ AGND	V	0.3 ~ -6.6
Supply voltage	VGH ~ AGND	V	-0.3 ~ +25
Supply voltage	VGL ~ AGND	V	0.3 ~ -16
Driver supply voltage	DDVDH – DDVDL	V	≦13.2V
Driver supply voltage	VGH – VGL	V	≦ 32.0V
Input voltage	V_{IN}	V	-0.3 ~ IOVCC + 0.3
HS Input voltage	V_{HSIN}	V	-0.3 ~ + 2
Operating temperature	Topr	℃	-30 ~ +70
Storage temperature	Tstg	℃	-55 ~ +110

Note:

Even if the one of the above parameters is exceeded momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the exceeding values which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

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13.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Operating voltage	VCI VCIP VCIR	-	2.5	2.8	3.6	V	
Operating voltage	IOVCC	-	1.65	1.8	3.6	V	Note1,2
OTP Supply voltage	VPP	-		5.0		V	Note1
Logic High level input voltage	V_{IH}	-	0.7*IOVCC		IOVCC	V	Note1
Logic Low level input voltage	V_{IL}	-	-0.3		0.3*IOVCC	V	Note1
Logic High level output voltage TE, SDO (SDA) , LEDPWM	V_{OH}	IOH = -1.0mA	0.8*IOVCC		IOVCC	V	Note1
Logic Low level output voltage TE, SDO (SDA) , LEDPWM	V_{OL}	IOL = +1.0mA	0		0.2*IOVCC	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18.0	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-8.0	V	
Driver Supply Voltage	-	|VGH-VGL|	16	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3
Source Driver							
Source Output Range	V_{SOUT}	-	VREG2OUT +0.1	-	VREG1OUT -0.1	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.0	-	6.1875	V	Note5
Negative Gamma Reference Voltage	VREG2OUT	-	-6.1875	-	-3.0	V	Note5
Source Output Setting Time	Tr	Below with 99% precision	-	15	20	us	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	30	mV	Note3
		4.2V>Sout>0.8V	-	-	20	mV	-
Output Offset Voltage	V_{OFFSET}	-	-	-	35	mV	Note3
Booster Operation							
Booster Voltage	DDVDH	-			6.5	V	
Booster Voltage	DDVDL	-	-6.5			V	
Booster Drop Voltage	DDVDH drop	loading=1mA	-	-	5	%	
Gate Driver High Voltage	VGH	-	8.0	-	18.0	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-8.0	V	
Standby mode current consumption							
Sleep In mode	$I_{(IOVCC\ SLP\ IN)}$	Ta = 25 °C VCI=2.8V IOVCC=1.8V	0	-	10	uA	
	$I_{(VCI\ SLP\ IN\ for\ DPI+SPI\ I/F)}$		5	-	60	uA	
	$I_{(VCI\ SLP\ IN\ for\ MIPI\ DSI\ I/F)}$		5	-	60	uA	
Deep Standby mode	$I_{(IOVCC\ DSTB)}$		0	-	1	uA	
	$I_{(VCI\ DSTB)}$		0	-	1	uA	

Note:

1. Ta = -30 to 70 °C (to 85 °C no damage), IOVCC=1.65V to 3.6V, VCIP=2.5V to 3.6V.
2. Supply digital IOVCC voltage equal or less than analog VCIP voltage.
3. Source channel loading = 10pF/channel
4. The Max. Value is between with Note 3 measure point and Gamma setting value
5. VREG1OUT≦DDVDH-0.3V and VREG2OUT≧DDVDL+0.3V.

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13.3. DSI DC Characteristics

DSI is using different state codes which are depending on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined on the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

Note: Ta=-30℃ to 70℃ (to +85℃ no damage)

13.3.1. DC characteristics for Power Lines

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Analog power supply voltage	VCI	Operating voltage	2.5	2.8	3.6	V
Digital power supply voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V
Analog power supply voltage noise	V_{VCI_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV
		Noise Range, 0 to 30kHz, Pulse Wave with Duty Cycle (50%/50%)	-	-	500	mV
I/O power supply voltage noise	V_{IOVCC_NOISE}	Noise Range, 0 to 100MHz, Sinusoidal Wave (peak-to-peak)	-	-	100	mV

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. These values are not symmetric amplitude, which centersm3g points are IOVCC or VCI. See examples as reference purposes, when V_{VCI_NOISE} and V_{IOVCC_NOISE} are maximums, below.

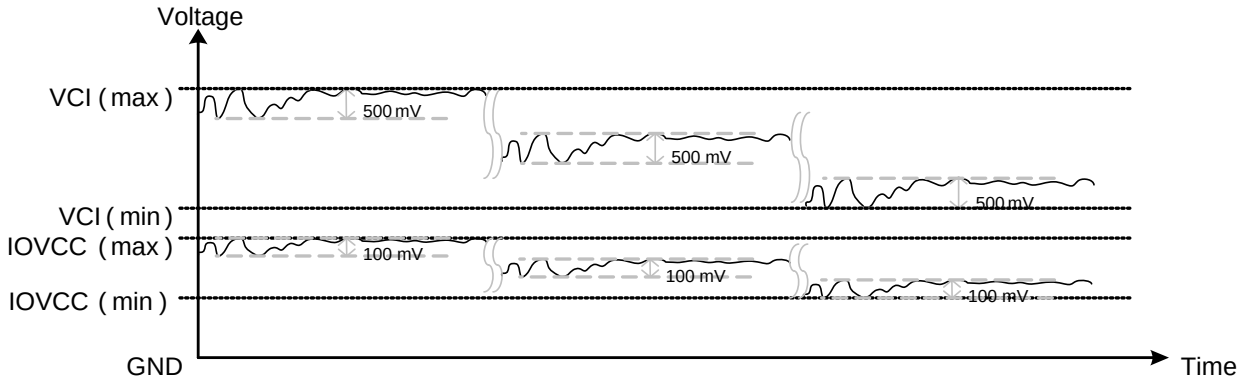


Figure 109 Noise on Power Supply Lines

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13.3.2. DC characteristics for DSI LP mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined on table below: DC Characteristics for DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned on the condition column. Other logical levels of the table are for MPU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic High level output voltage	V_{OH}	I_{OUT}=-1mA, Note 2	0.8 V_{IOVCC}	-	V_{IOVCC}	V
Logic Low level output voltage	V_{OL}	I_{OUT}=1mA, Note 2	0.0	-	0.2V_{IOVCC}	V
Logic High level input voltage	V_{IHLPCD}	LP-CD, Note 3	450	-	1350	mV
Logic Low level input voltage	V_{ILLPCD}	LP-CD, Note 3	0.0	-	200	mV
Logic High level input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1), Note 3	880	-	1350	mV
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1), Note 3	0.0	-	550	mV
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode), Note 3	0.0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0), Note 3	1.1	-	1.3	V
Logic Low level output voltage	V_{OLLPTX}	LP-TX (D0), Note 3	-50	-	50	mV
Logic High level input current	I_{IH}	LP-CD, LP-RX, Note 3	-	-	10	uA
Logic Low level input current	I_{IL}	LP-CD, LP-RX, Note 3	-10	-	-	uA

Note:

1. Ta=-30℃ to 70℃ (to +85℃ no damage)
2. LEDPWM
3. DSI High Speed mode is off

13.3.3. Spike / Glitch Rejection

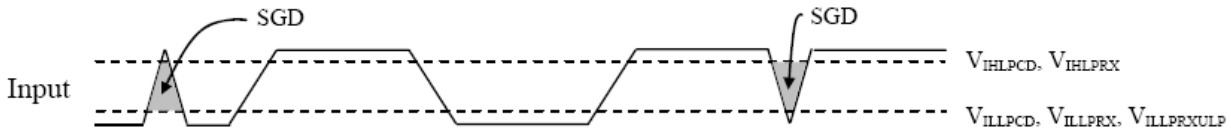


Figure 110 Spike / Glitch Rejection

Note:

1. Peak Interference Amplitude max. 200mV and Interference Frequency min. 450MHz.
2. n = 0 and 1.

Table 44 Spike / Glitch Rejection

Spike / Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-, DSI-Dn+/-	SGD	Input pulse rejection for DSI	-	300	Vps

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13.3.4. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	DSI-CLK+/- Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DSI-Dn+/- Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	DSI-CLK+/- Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DSI-Dn+/- Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	DSI-CLK+/-	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DSI-Dn+/- Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	DSI-CLK+/-	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DSI-Dn+/- Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	DSI-CLK+/-	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DSI-Dn+/- Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/- Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/- Note 5, Note 6	-	-	60	pF

Note:

1. Ta = -30℃ to 70℃ (to +85℃ no damage), IOVCC = 1.65 to 1.95V.
2. Includes 50mV (-50mV to 50mV) ground difference.
3. Without VCMRCLKM450/VCMRDATAM450.
4. Without 50mV (-50mV to 50mV) ground difference.
5. n = 0 and 1.
6. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

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The DSI receiver (HS mode) is understanding that there is logical '1' (HS-1) when a differential voltage is more than V_{THH} (CLK+/DATA+) and the DSI receiver (HS mode) is understanding that there is logical '0' (HS-0) when a differential voltage is more than V_{THL} (CLK-/DATA-). There is undefined state if the differential voltage is less than V_{THH} (CLK+/DATA+) and less than V_{THL} (CLK-/DATA-). A reference figure is below.

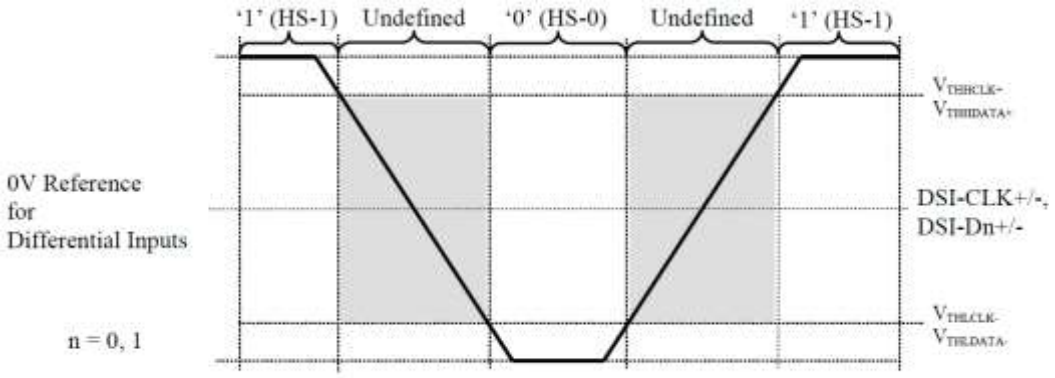
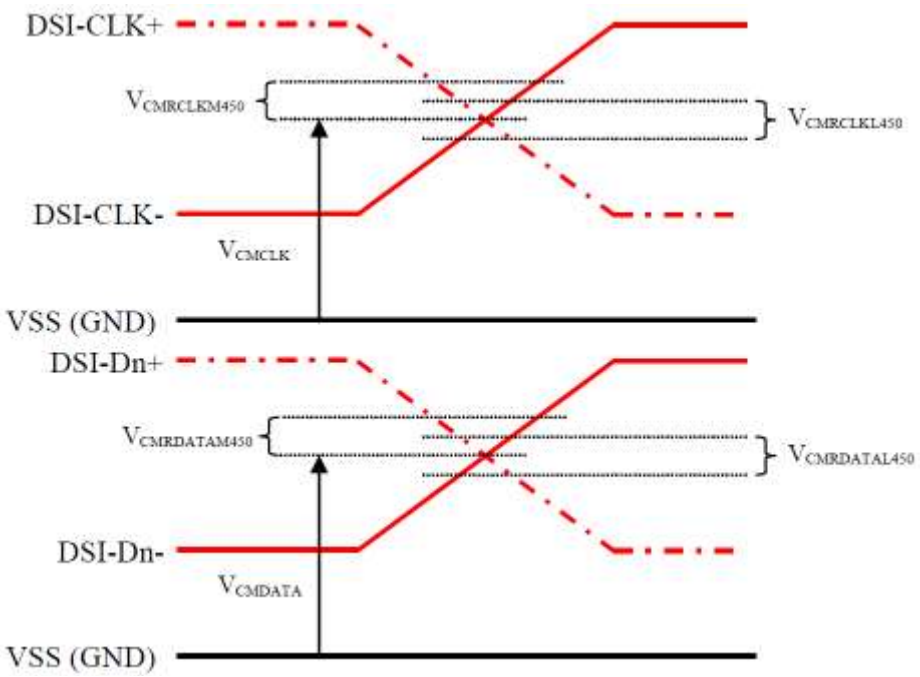


Figure 111 Differential Inputs Logical '0's and '1's, Threshold High/Low, Differential Voltage Range



Note: n = 0 and 1

Figure 112 Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (DSI-CLK+ ⇔ DSI-CLK- or DSI-D0+ ⇔ DSI-D0- or DSI-D1+ ⇔ DSI-D1-)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (DSI-CLK+ ⇔ DSI-CLK- or DSI-D0+ ⇔ DSI-D0- or DSI-D1+ ⇔ DSI-D1-)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

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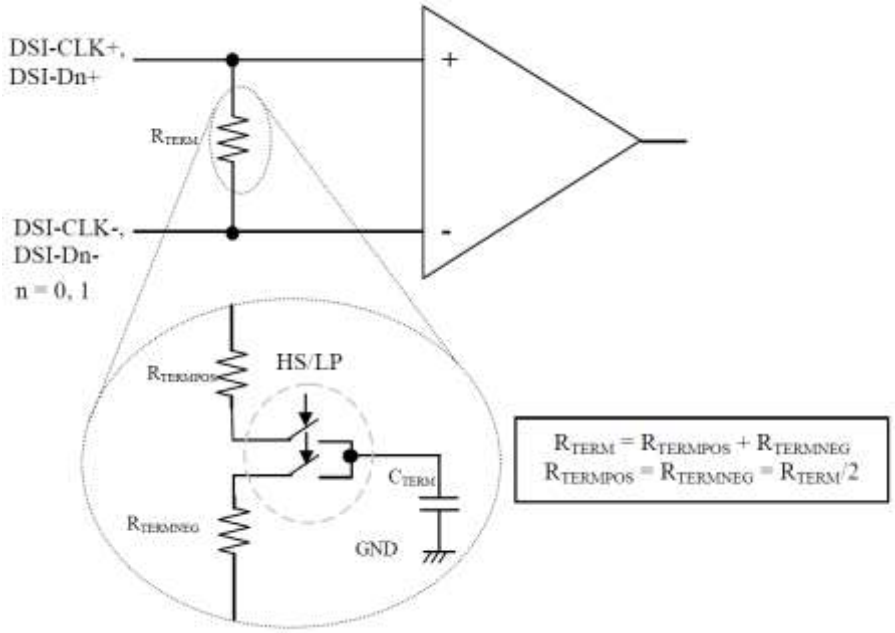
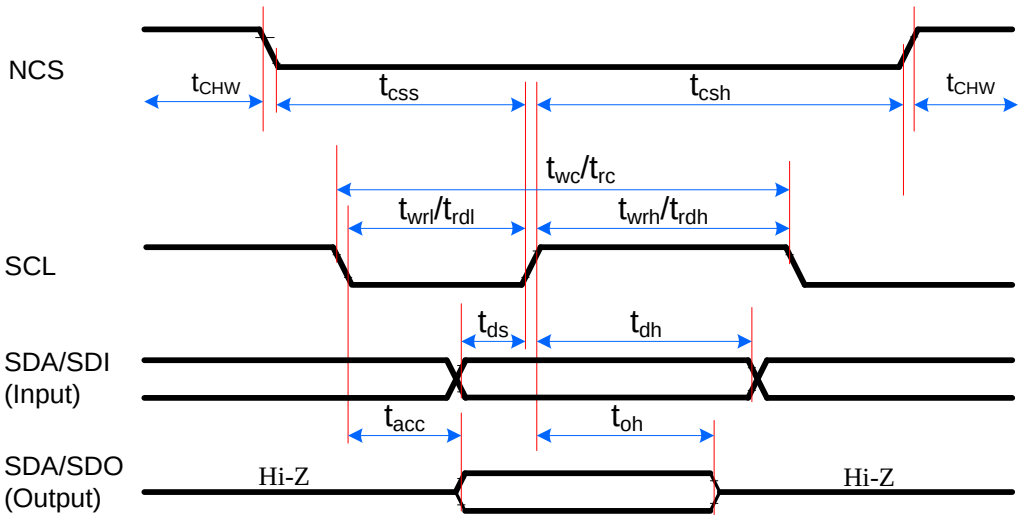


Figure 113 Differential Pair Termination Resistor on the Receiver Side

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13.4. AC Characteristics

13.4.1. Display Serial Interface Timing Characteristics (3-line SPI system)



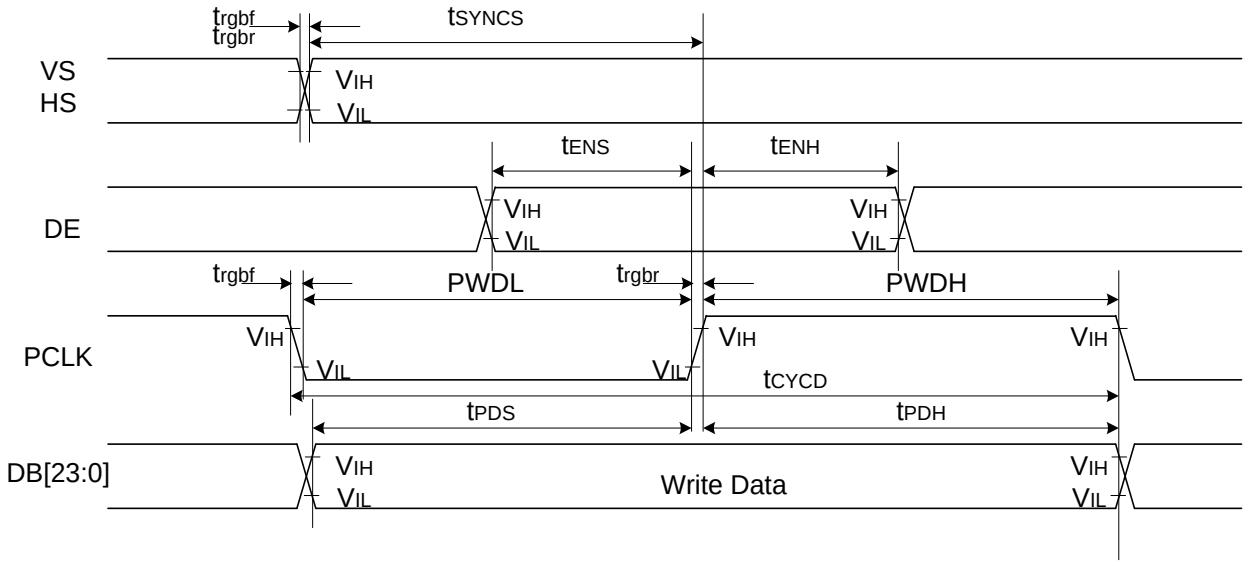
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS “H” pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL “H” pulse width (Write)	10	-	ns	
	twrl	SCL “L” pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

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13.4.2. Parallel 24/18/16-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V

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13.4.3. DSI Timing Characteristics

13.4.4. High Speed Mode – Clock Channel Timing

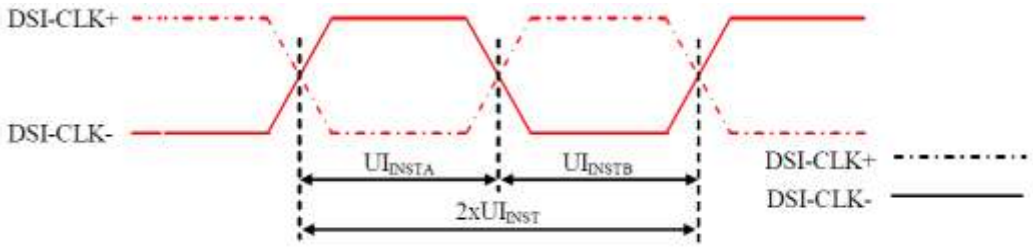


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: UI = UI_{INSTA} = UI_{INSTB}

13.4.5. High Speed Mode – Data Clock Channel Timing

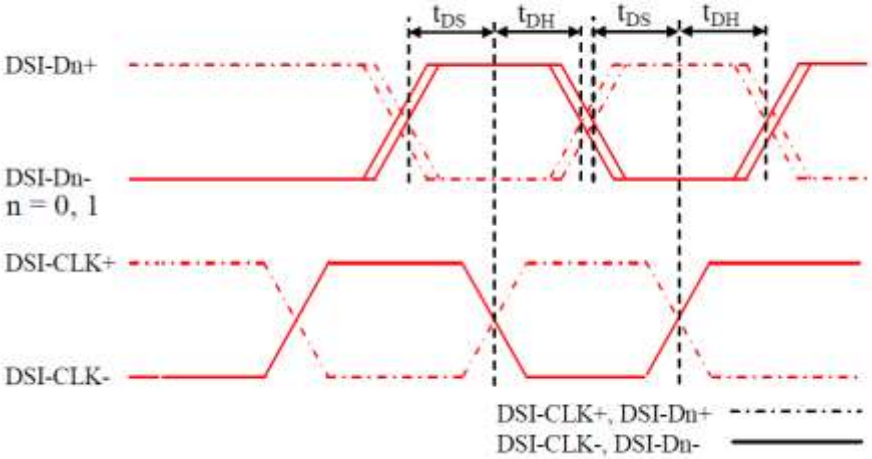


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

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13.4.6. High Speed Mode – Rise and Fall Timings

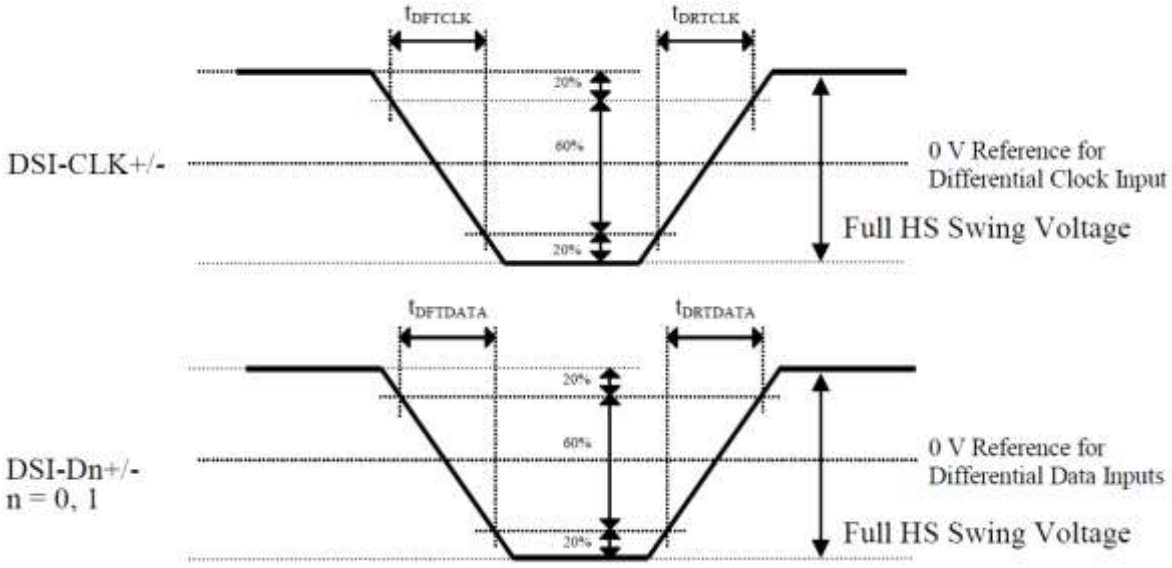


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150	-	0.3UI (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	150	-	0.3UI (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150	-	0.3UI (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	150	-	0.3UI (Note)	ps

Note:The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard

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13.4.7. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI9806E-2C) sequence below.

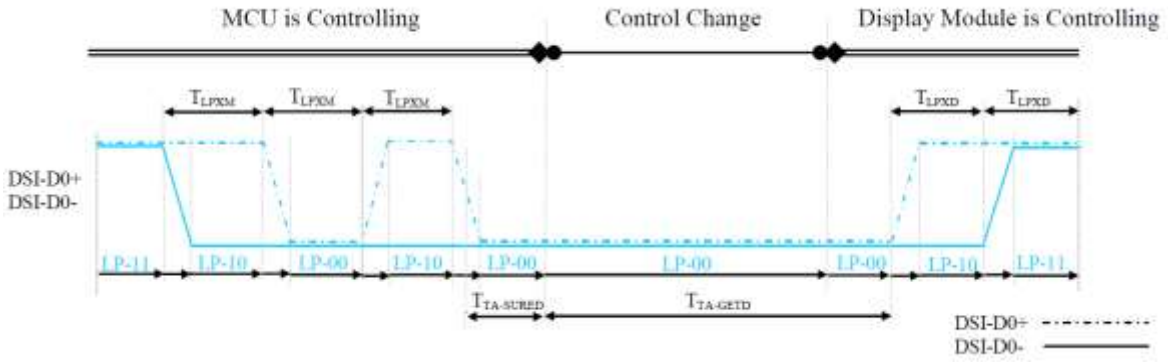


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (ILI9806E-2C) to the MPU sequence below.

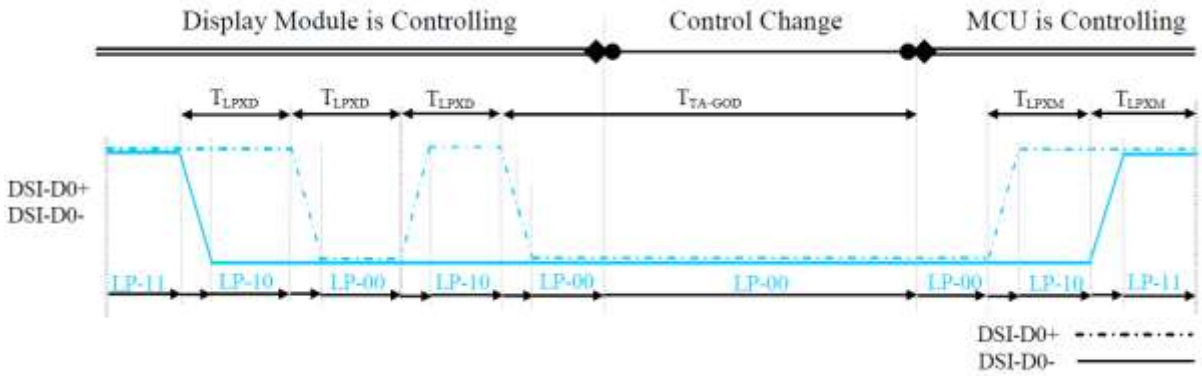


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU ➔ Display Module (ILI9806E-2C)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9806E-2C) ➔ MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI9806E-2C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9806E-2C)	$5 \times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4 \times T_{LPXD}$	ns

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13.4.8. Data Lanes from Low Power Mode to High Speed Mode

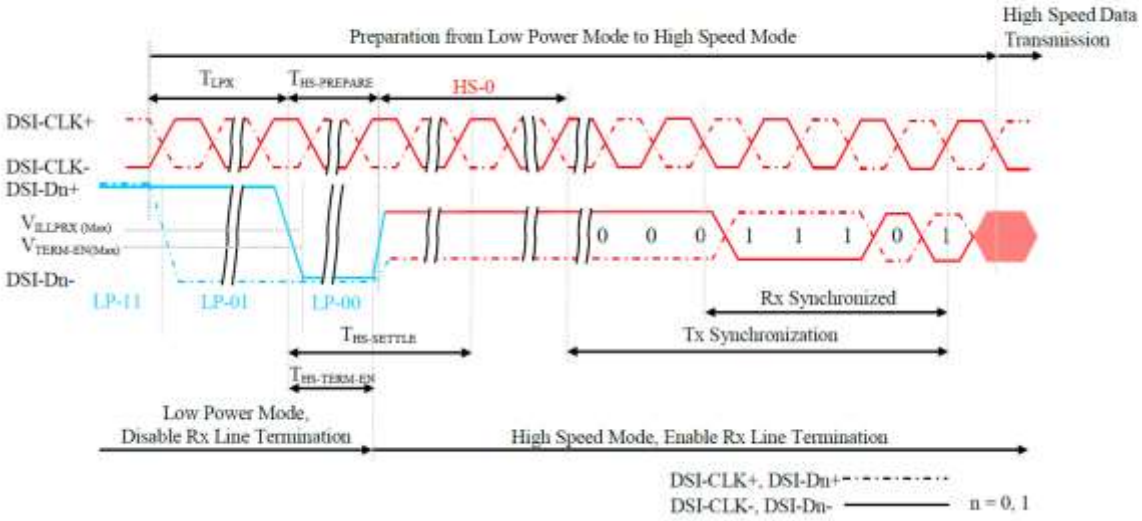


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

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13.4.9. Data Lanes from High Speed Mode to Low Power Mode

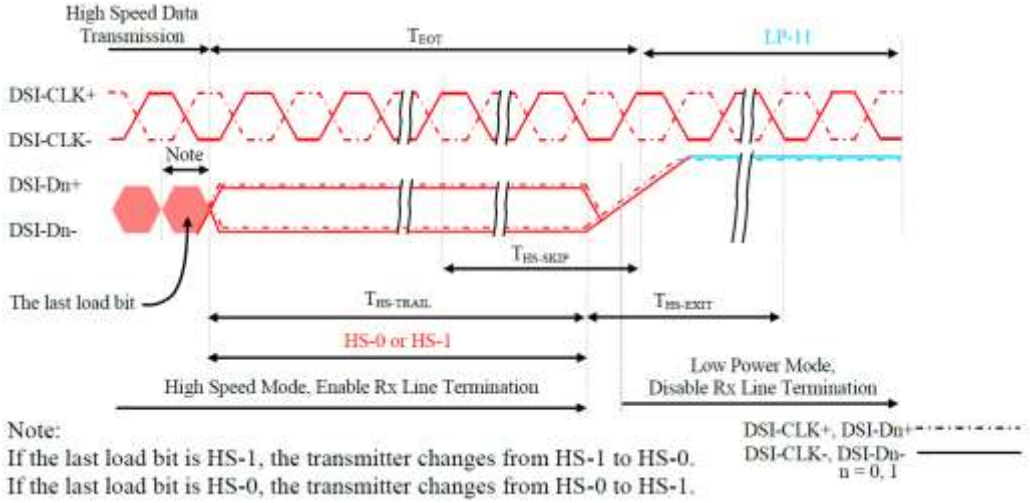


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9806E-2C) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

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13.4.10. DSI Clock Burst – High Speed Mode to/from Low Power Mode

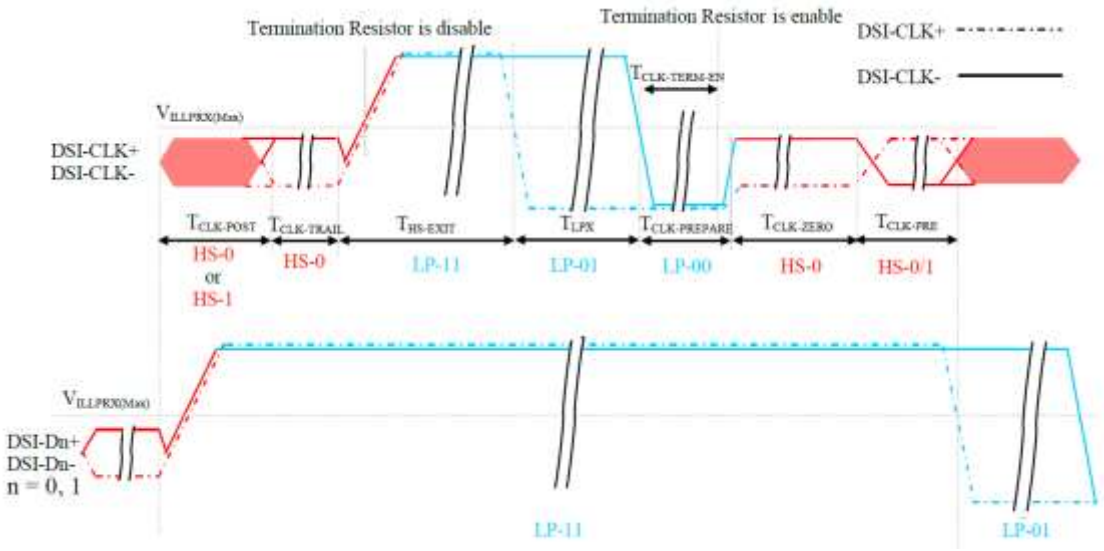


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

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14. Application Circuit

14.1. Reference Circuit

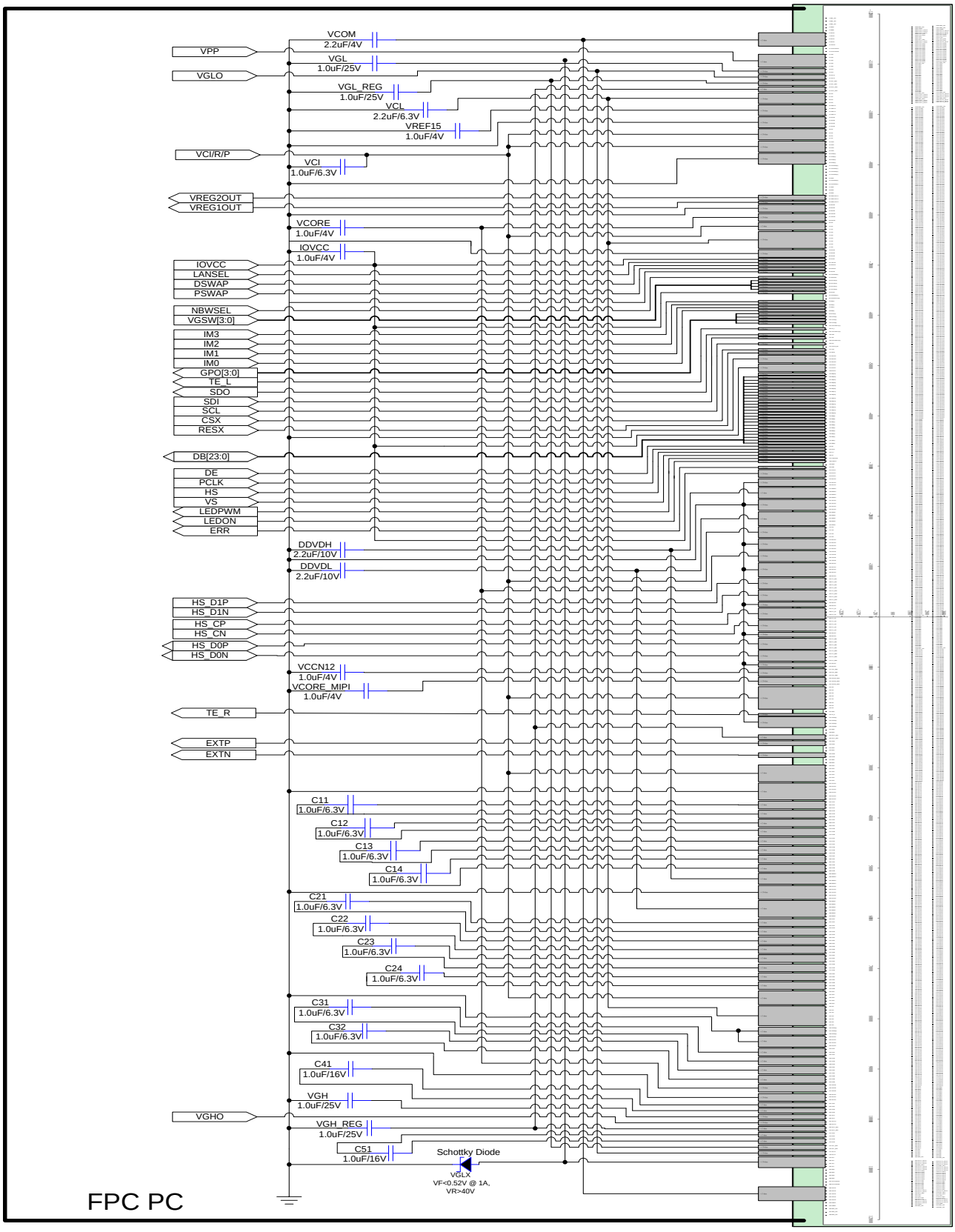


Figure 122 Reference Circuit

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14.2. ILI4002/ILI4003 Application Circuit

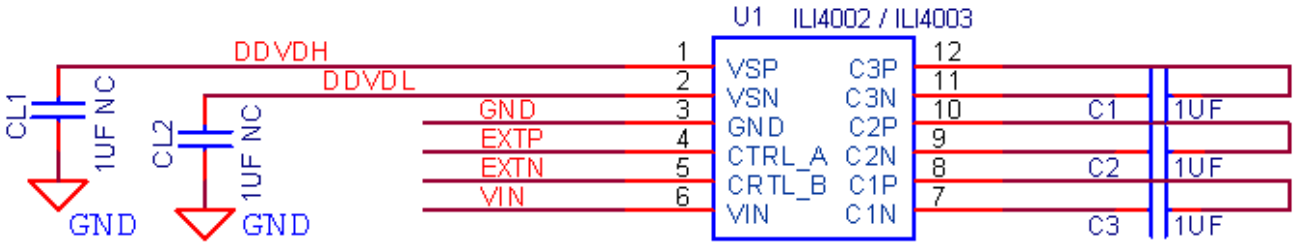


Figure 123 ILI4002/ILI4003 Reference Circuit

Table 53 ILI4002/ILI4003 External Component

Cap.	Value
CL1	1uF (Min 10V)
CL2	1uF (Min 10V)
C1	1uF (Min 10V)
C2	1uF (Min 10V)
C3	1uF (Min 10V)

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14.3. External Component

The Table 54 shows specifications of external elements connected to the power supply circuit of ILI9806E-2C.

Table 54 External Component table

Pad Name	Connection	Typical Value
IOVCC	Stable Capacitor to GND	1.0 µF (Min 4.0V) (Option[Note 1])
VCI, VCIP, VCIR	Stable Capacitor to GND	1.0 µF (Min 6.3V)
VCORE	Stable Capacitor to GND	1.0 µF (Min 4.0V)
VCORE_MIPI	Stable Capacitor to GND	1.0 µF (Min 4.0V)
V12_MIPI	Stable Capacitor to GND	1.0 µF (Min 4.0V)
C11P, C11N	Flying Capacitor	1.0 µF (Min 6.3V)
C12P, C12N	Flying Capacitor	1.0 µF (Min 6.3V)
C13P, C13N	Flying Capacitor	1.0 µF (Min 6.3V)
C14P, C14N	Flying Capacitor	1.0 µF (Min 6.3V) (Option[Note 2])
C21P, C21N	Flying Capacitor	1.0 µF (Min 6.3V)
C22P, C22N	Flying Capacitor	1.0 µF (Min 6.3V) (Option[Note 2])
C23P, C23N	Flying Capacitor	1.0 µF (Min 6.3V)
C24P, C24N	Flying Capacitor	1.0 µF (Min 6.3V) (Option[Note 2])
C31P, C31N	Flying Capacitor	1.0 µF (Min 6.3V)
C32P, C32N	Flying Capacitor	1.0 µF (Min 6.3V) (Option[Note 2])
C41P, C41N	Flying Capacitor	1.0 µF (Min 16V)
C51P, C51N	Flying Capacitor	1.0 µF (Min 16V)
DDVDH	Stable Capacitor to GND	2.2 µF (Min 10V)
DDVDL	Stable Capacitor to GND	2.2 µF (Min 10V)
VCL	Stable Capacitor to GND	2.2 µF (Min 6.3V)
VGH	Stable Capacitor to GND	1.0 µF (Min 25V)
VGL	Stable Capacitor to GND, VGLX=VGL	1.0 µF (Min 25V)
	Schottky Diode to GND	VF < 0.52V @ 1A, VR > 40V (Option)
VGL_REG	Stable Capacitor to GND	1.0 µF (Min 25V) (Option[Note 3])
VGH_REG	Stable Capacitor to GND	1.0 µF (Min 25V) (Option[Note 3])
VCOM	Stable Capacitor to GND	2.2 µF (Min 4.0V)
VREF15	Stable Capacitor to GND	1.0 µF (Min 4.0V)

Notes

1. **Remove the capacitor when MIPI IF is in use.**
2. **Remove the capacitor, the DDVDH Voltage must be set to VCI X2, DDVDL Voltage must be set to VCI X-3, and VCL Voltage must be set to VCI X-1.**
3. **Remove the capacitor when not in use.**
4. **The application of table is based on panel's loading.**

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15. Revision History

Version No.	Date	Page	Description
V090	2013/06/28	All	New created.
V091	2013/07/09	221	Modify the TOUCH_OPT[1:0] Table
		310	Remove the Diode option of DDVDH
V092	2013/08/06	177	Modify the description of P0_RFEh register
		184	Modify the default value (P1_R21h=01h)
		199	Modify the default value (P1_R41h=22h)
		219	Modify the default value (P1_R57h=20h)
		220	Modify the default value (P1_R58h=90h)
		259	Add the restriction of LABC_SRE_THR function
		137 & 260	Add the SRE Control register
		137 & 261	Add the ALS function register
		138~139 & 264~265	Add the GIP Setting register
		139 & 266	Add the GOUT_VGLO control register
		139 & 267	Add the GOUT_VGHO control register
		140 & 268	Add the VCL control register
		140 & 269	Add the VGL_REG enable register
		140 & 270	Add the VREG1OUT and VREG2OUT enable register
		271	Modify the Figure 95
		284	Add the description of internal programming in Note2
V093	2013/08/26	17 & 193	Remove the 1/3/4 dot Inversion function
V094	2013/09/12	22	1. Modify description “Fix to IOVCC or DGND level when not in use” for the CSX & SCL & SDI(SDA) input pin 2. Modify description “Fix to IOVCC , DGND or Floating level when not in use” for the DB[23:0] input pin
		29	Modify the Output PAD of 2.5. Bump Arrangement
		50	Table 10, CLOCK_P modify to Control mode, CLOCK_N modify to Escape mode
		141~176	Add the description at Restriction
		219	Modify the values of VDET set
		257	Modify the value of DIM_MOV/STILL[2:0] table
		258	Modify the value of DIM_UI[2:0] table
		264	Add the description of F_TIME_OPT function
		267	Add the register of P6_R52h
		268	Modify the register name
		270	Add the register of P7_R02h
		280	Remove the 8.2. Gamma Default Values(for NW type LC)
		309	Modify the SLP-IN current for DPI+SPI I/F, and add the SLP-IN current for MIPI DSI I/F
		310	Modify the table of Line DC Voltage Levels
V095	2013/10/30	48	1. Modify the Max. value of DCLK , 41.7MHz modify to 35.7MHz 2. Modify the ”Note1. HLW+HBP+HFP >= 4.5us”
		274	Add the TIME CONTROL(Page7_RE1h) register
		324	Modify the Figure 122 and add the ITO resistance of input pad
V096	2014/01/15	231	Modify the Program / Read address table
V097	2014/03/24	311	Modify the Max. & Min. current for Sleep-In & Deep Standby
V098	2014/04/07	23	MIPI swap pin table updata as IC pad sequence
V099	2014/06/13	26	Add “Fix to DGND level when not in use.” in VPP pin description
		137	Add the table of Color Enhacement
		264	Add the register(P5_R1Ah) of Color Enhacement
		283	Modify the Figure99 and add the notes
		284	Modify the Figure100 and add the note
		328	Modify the connection from EXTP & EXTN to CTRL_A&B of the Figure 124
		329	Add options of C13 & C14 & C22 & C24 & C32 & VGH/L_REG and append notes to describe it.
V100	2014/06/26	283	Modify timing of the trPWRESEX in Figure99
		329	Modify the Table 53. The option of C13 changes to IOVCC, and append note to describe it.
V101	2014/09/23	313	Modify the VGH/VGL values
		329	Modify the cap value of VCORE
V102	2015/01/23	282	Modify the chapter 7. Power ON/OFF Sequence figure and add note
		294~309	Modify the Gamma Table
		310~311	Add the Deep Standby Entry/Exit Sequence Flow Chart
		312	Modify the figure 111 Deep Standby Mode Entry / Exit

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		317	Modify the 14.3.2 DC characteristics for DSI LP mode
		324	Modify the Table 47 Rise and Fall Timings on Clock and Data Channels
V103	2015/10/20	264	Remove the P5_R1Ah register fnction
		265~266	Remove the P5_R25h~P5_R3Ch register fnction
		268	Add the P6_R54h_D[3:0] register function
		269	Add the P7_R00h register function
		274	Add the P7_RB3h register function
		278~279	Remove the 5. Color Enhancement function description

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